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Design and Investigation of an FPGA-Based Data Acquisition and Control Architecture With MRI RF Interference Reduction Capabilities for Simultaneous PET/MRI Systems

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Design and Investigation of an FPGA-Based Data Acquisition and Control Architecture With MRI RF Interference Reduction Capabilities for Simultaneous PET/MRI Systems

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Thesis abstract

The combination of Positron Emission Tomography (PET) and Magnetic Resonance Imaging (MRI) as a multi-modality imaging technique allows the simultaneous acquisition of information about metabolic processes with very sensitivity from PET, and high-resolution anatomical or functional MR images with an excellent soft-tissue contrast from MRI. However, the design of PET/MRI systems providing an unaffected PET and MRI performance during simultaneous operation is challenging. An integration and operation of PET with a large field of view for clinical whole-body imaging can be realised through the use of semiconductor-based photo-detectors which are MR-compatible and very small compared to conventional photo-detectors. PET systems based on these new photo-detector require a dramatically higher, typically two orders of magnitude, number of detector channels to be read out by the PET acquisition system. The latter are usually designed for particular systems and are not based on architectural approaches to be easily adaptable to different detector configurations. The first aim of this thesis was to conceive a PET data acquisition architecture with concepts offering a high level of flexibility in order to meet the requirements of current and future, preclinical and clinical PET and PET/MRI detector configurations using semiconductor photo-detectors. This architecture was implemented for two preclinical PET inserts, Hyperion I and Hyperion II^D, designed for simultaneous PET/MRI. The second system uses the latest detector technology known as the digital SiPM (made by Philips). The PET data acquisition platform design for Hyperion II^D as well as investigations in the data transmission stability under different PET and PET/MRI operating conditions are presented.

PET detectors operated in an MRI bore commonly use radio-frequency (RF) shielding to reduce PET-related RF interference and hence preserve the MR image quality. However, shields require conducting materials which give rise to

eddy currents within the switching MRI fields. These eddy currents lead to local MRI field disturbances and thus MR image artefacts. The drawbacks could be avoided by operating a PET system without RF shielding, which would, however, require the PET system not to couple spurious RF signals into the MRI RF signal receive coil. The second objective of the thesis was therefore to exploit the novel capabilities of the new data acquisition system and modify the RF emissions from the PET electronics in such ways that the RF noise coupling into the MRI coil can be lowered. Three different RF interference reduction (IR) techniques are proposed which are based on firmware of field-programmable gate array (FPGA) devices, thereby offering RF IR modifications at any time compared to permanently mounted PET shields. The techniques were studied by performing simulations PET and MRI measurements. The thesis closes with PET/MRI *in vivo* and *ex vivo* measurement results to demonstrate the feasibility and stability of the data acquisition system and the imaging capabilities of Hyperion II$^{\mathrm{D}}$.

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Chapter 1

Introduction

1.1 Hybrid PET/MR imaging

Positron emission tomography (PET) is an imaging modality used for functional imaging in nuclear medicine. It allows many biochemical processes to visualised non-invasively at a very high sensitivity (detectability is in the picomolar range) by detecting gamma radiation emitted from a biomarker that is labelled with a positron-emitting radio-nuclide. The radio-tracer, is administered to the patient, distributes in the body and targets the metabolic processes of interest. The tracer distribution can be quantified with PET which is used, for example, to assess the disease response during therapy.

PET, however, provides images with a low spatial resolution ($4-6\,\mathrm{mm}$ for current clinical PET systems) and lacks anatomical information. Therefore, by combining PET with X-ray *computed tomography* (CT) or *magnetic resonance imaging* (MRI), the radio-tracer distribution can be localized. In the late 1990s, the first single device combining PET and CT was presented [1] and the added value of CT was demonstrated in clinical studies thanks to the more accurate localisation of physiological legions [2, 3, 4]. The anatomical information from CT is obtained, however, at the expense of ionising radiation which adds to the gamma radiation of the PET tracer. Moreover, CT has a poor soft-tissue contrast and can only be operated sequentially with PET. Compared to CT, MRI provides an outstanding soft-tissue contrast, does not use ionising radiation and can in principle be operated simultaneously with PET. The latter enables a precise spatial and temporal

correlation of PET and MRI data. This is particularly of interest for thorax and cardiovascular PET/MR imaging, where PET images can be corrected for moving and respiratory artefacts using MRI information to motion-correct and thus improve PET images. Besides high-resolution anatomical imaging (approx. 1 mm), functional imaging such as spectroscopy-, perfusion- or diffusion-imaging can be performed with MRI which can add further complementary information to PET. Combined PET/MRI is of high interest for oncology, neurology, cardiovascular and paediatric imaging. [5, 6, 7, 8, 9, 10].
Since the 1990s, substantial research and development of software-based medical image processing (e.g. image fusion) and of devices combining hardware of different imaging modalities has been developed to explore and use the benefits of multi-modal imaging within modern medicine. Multi-modality imaging with PET/CT has become indispensable, because it can improve the clinical workflow, and complementary information obtained by functional and anatomical imaging improves diagnostic accuracy. Better lesion detection and localisation can decrease the possibility of ambiguous diagnostic results, or failed diagnosis due to undetected anomalies. Improvements in the accuracy with which biomarker uptake can be quantified have led to better monitoring of treatment response, and multi-modality imaging allows accelerated protocols which raises the patient ease during examination [11, 12]. Combined imaging techniques are also increasingly used to study biochemical processes in the field of drug or imaging biomarker development in the domain of preclinical as well as clinical research.

1.2 PET/MRI system design challenges

The first descriptions of the design and successful demonstration of simultaneous PET/MR imaging were reported in the mid 1990s [13, 14] before PET was combined in a single device with CT. From a technological point of view, the integration of PET detectors into an MRI system is much more challenging than construction of sequential PET/CT. Besides the fact that the PET detectors have to be integrated in a spatially limited MRI bore, laborious measures need to be taken to ensure a proper operation of PET and MRI. Any materials placed into the MRI can result in magnetic field distortions, and PET-related electronics

have the ability to couple unwanted radio-frequency (RF) signal emitted by PET into the MRI RF receive chain. Both effects lead to MR image quality deterioration. The magnetic and RF-fields generated by an MRI can either lead to inoperable electronic circuits in PET detectors or disturb their operation to yield an impairment of the PET image quality. To avoid these mutual interferences, PET detectors need to be designed in such a way that they are *MR-compatible* so that the imaging performance of both PET and MRI is preserved.

As the conventional PET photo-detector technology, the *photo-multiplier* (PMT), is bulky and does not operate within magnetic fields, semi-conductor-based, small-sized sensors such as *avalanche photo-diodes* (APD) and *silicon photo-multipliers* (SiPM) developed during the last two decades have been explored as an alternative. They have proven to be MR-compatible, allow for highly integrated PET detectors, and several preclinical PET/MR imaging prototype systems and three clinical PET systems have so far been designed using APDs or SiPMs. Due to the small size of the sensors, PET data acquisition systems have to acquire data from higher number of detector channels compared to the number typically found in PMT-based systems. This is particularly the case for clinical PET systems: For instance, the data acquisition system of the Philips PMT-based PET/CT system Gemini TF acquires detector data from 420 channels [15], whereas the recently announced Philips Veros based on *digital SiPMs* (dSiPM) needs 23040 channels [16] to be read out. With the new SiPM-based system, the channel number has been increased by two orders of magnitude.

The design of PET detectors for simultaneous PET/MR image acquisition without a deterioration in image quality has been an active field of research for two decades. Most of the reported MR-compatible PET systems transfer the analogue detector signals via cabling away from the strong magnetic fields towards data acquisition electronics in order to digitize and process the detector signals. However, PET signals transmitted over long cables tend to experience MRI-related RF interference which degrades the PET performance. Moreover, designing a clinical detector configuration using this approach would yield a very large amount of cabling and is thus limited in scalability.

Another possibility is to digitize the detector data locally in the MRI as close as possible to the detectors. This reduces the possibility of MRI fields interfering with analogue PET signals. To demonstrate the feasibility of localised

PET digitisation using SiPMs while preserving the MRI image quality, a prototype MR-compatible PET insert (named Hyperion I) designed to fit into a clinical 3-T MRI was developed in the scope of the European FP7 HYPERimage project.

1.3 PET data acquisition architecture for SiPM-based PET detectors

The first aim of this thesis was to conceive and design a data acquisition system with sufficient resources to acquire data from 3840 SiPM sensor channels. The acquisition platform was required to have extensive flexibility to support all kinds of research activity planned with the PET insert. As future research relating to the development of clinical PET/MR systems with highly-integrated PET detectors was planned, one of the tasks was to conceive a scalable and modular data acquisition architecture with support for any kind of current and future PET and PET/MRI detector configurations.
Encouraged by the promising PET/MRI performance results obtained with the Hyperion I insert, a follow-up PET insert (named Hyperion II^{D}) was built. Compared to Hyperion I which uses analogue SiPMs in combination with application-specific integrated circuits for digitization purposes, the new insert is based on fully digital SiPMs (from Philips Digital Photon Counting) which represent the latest step in the evolution of semiconductor-based photo-detectors for PET. Digital SiPMs perform the PET signal digitisation internally and hence output digital data instead of analogue signals. Further tasks of the thesis addressed the adaptation of the data acquisition platform implemented for Hyperion I to the new requirements of the follow-up PET system with dSiPMs and investigations in the data transmission stability of the Hyperion II data acquisition platform.

1.4 MRI RF interference reduction for simultaneous PET/MRI

Generally, the preservation of PET signal quality via local digitization occurs at the expense of having to move large amounts of electronics inside the MRI. Switching signals with steep slopes and periodically switching signals as performed by clocked electronics tend to emit RF fields which can couple into the MRI RF receive chain via the RF receive coil. This unwanted, spurious signal coupling reduces the MRI signal *signal-to-noise* (SNR) which results in deteriorated image quality. A common way of reducing interferences caused by PET detectors is to enclose them with shielding material. This non-trivial task of designing RF shields for PET is usually done during the development phase of PET detectors for PET/MRI and is a non-changeable part of a detector. Shielding materials are conductors which can locally disturb the MRI magnetic fields and hence impair MR image quality. The second aim of this thesis addressed the PET-related RF interference reduction by investigating techniques supported by the data acquisition platform with the aim of minimising PET RF shielding or removing it altogether.

1.5 Thesis objectives and structure

The objectives of the thesis were the following:

1. To conceive a scalable and modular data acquisition architecture for PET systems which can address the requirements of current and future semiconductor-detector-based detector configurations for preclinical and clinical PET.

2. To design and implement the newly conceived architecture for the Hyperion I and Hyperion II^{D} which both use different detector technologies. In this thesis, the implementation for the latter system is presented and investigations of the data transmission stability for different PET and PET/MR operating conditions are studied.

3. To investigate novel PET-related RF interference reduction techniques made possible with the data acquisition platform. Different approaches had to be explored with regard to their implementation feasibility and their effectivenss in terms of RF interference reduction:

    - An MRI-synchronous PET data acquisition gating technique aiming at an RF interference reduction by interrupting the PET DPC sensor operation during MRI RF signal acquisition phase.
    - Shifting the clock frequency of the PET DPC sensors in such ways that the modified electromagnetic field spectra emitted by the PET module and coupled into the MRI RF receive chain reduce the PET-related RF interferences.
    - Phase-shifting the clock signals of PET DPC sensors to each other so that the resulting changed electromagnetic field emission lowers the noise coupled into the MRI RF receive chain.

The first section of chapter 2 gives an introduction to the fundamental principles and limitations of PET which is followed by an overview of PET detector technology and associated terminologies. The next section introduces the reader to PET imaging requirements which have a direct impact on the performance

requirements of a PET data acquisition system. It follows an overview on state-of-the-art acquisition systems and an introduction to the data processing technologies used here, in particular the *field-programmable gate array* (FGPA). FPGA basic principles and advantages are introduced, as these relate to the data acquisition architecture of the Hyperion PET inserts. Some requirements of the Hyperion data acquisition systems are also MRI-related since the inserts aim at simultaneous PET/MR imaging. Hence, an introduction to basic principles of MRI are given in the next section, followed by a brief overview of combined PET/MRI and the different types of interference between PET and MRI. Afterwards, the reader is introduced to terminology and principles related to RF interference reduction approaches. Finally, the Hyperion I and Hyperion II^D PET inserts and their system requirements are described which determine the specifications for their data acquisition systems.

In chapter 3, the concepts of the new data acquisition architecture are described in detail. This is followed by an overview of the acquisition system requirements derived from the needs of the Hyperion II^D insert. Then, the reader is introduced to the actual design. The last part of the chapter deals with investigations of the data transmission stability through measurements performed under different PET and PET/MRI operating conditions.

Chapter 4 represents the first of three chapters dealing with the topic of PET-related RF interference reduction. In chapter 4, a technique is presented to reduce RF interference via the concept of PET data acquisition gating. A new method required to make the dSiPMs of the PET insert suitable for the gating approach is introduced and an assessment of the suitability of PET gating with regard to a fractional PET sensitivity loss for different MRI sequences is presented. Finally, the reduction technique is evaluated by performing MRI measurements.

Chapter 5 introduces the reader to the concept of RF interference reduction through the changing of clock frequencies used by the PET electronics and the dSiPMs. The impact of the frequency changes on the RF fields emitted by PET electronics are evaluated on a lab bench measurement setup as well as by performing MRI measurements.

Chapter 6 completes the interference-reduction-related investigations by proposing an RF reduction through clock phase shifting. This method is introduced with simulations for different clock phase patterns and closes with MRI measure-

ments using a Hyperion II^D PET module.
The chapter closes with a comparison on the presented different RF interference reduction techniques and outlines their advantages and disadvantages, and which technique is best suited depending on the aimed applications. Initial *in vivo* and *ex-vivo* PET/MR imaging results performed with the dSiPM-based insert are presented in chapter 7. The images demonstrate the operational stability and the *in vivo* capabilities of the system when performing simultaneous PET/MR mouse imaging.
The thesis closes with a discussion on the conclusions which can be drawn from the work and gives suggestions for future research.

1.6 Contribution in the thesis

This thesis is the work of the candidate. Particular areas where others have contributed specialist input are listed in the following.
The FEM simulation and Matlab calculation results presented in chapter 6 were performed by Jakob Wehner. He also helped to set up the lab bench measurement protocol used to acquire the broadband frequency spectra and the field pattern measurements for chapters 5 and 6 and generated the MRI noise and SNR plots, and the field maps shown in chapters 4 to 6.
The PET singles and coincidence processing software as well as the PET raw data acquisition running on the data acquisition and processing server was implemented by Benjamin Goldschmidt. Dr. André Salomon developed the software to reconstruct the PET images presented in chapter 7.

1.7 List of publications

1.7.1 Peer-reviewed journal papers

1. Gebhardt, P, Wehner, J., Weissler, B., Frach, T., Marsden, P.K. and Schulz, Volkmar. RESCUE - Reduction of MRI SNR Degradation by Using an MR-Synchronous Low-Interference PET Acquisition Technique. In: *Nuclear Science, IEEE Transactions on* 62.3 (2015), pp. 634 643. doi : 10.1109/TNS.2015.2434851.

2. Gebhardt, P, Wehner, J, Weissler, B, Botnar, R, Marsden, PK and Schulz, V. FPGA-based RF interference reduction techniques for simultaneous PET-MRI. In: *Physics in Medicine and Biology* 61.9 (2016), p. 3500. doi : 10.1088/0031-9155/61/9/3500.

3. Wehner, Jakob, Weissler, Bjoern, Dueppenbecker, Peter, Gebhardt, Pierre, Schug, David, Ruetten, Walter, Kiessling, Fabian and Schulz, Volkmar. PET/MRI insert using digital SiPMs: Investigation of MR-compatibility. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 734 (2014), pp. 116121. doi : 10.1016/j.nima.2013.08.077.

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7. Weissler, Bjoern, Gebhardt, Pierre, Lerche, Christoph W, Soultanidis, Georgios M, Wehner, Jakob, Heberling, Dirk and Schulz, Volkmar. PET/MR Synchronization by Detection of Switching Gradients. In: *Nuclear Science, IEEE Transactions on* 62.3 (2015). doi : 10.1109/TNS.2015.2427995.

8. Goldschmidt, Benjamin, Schug, David, Lerche, Christoph, Salomon, Andre, Gebhardt, Pierre, Weissler, Bjoern, Wehner, Jakob, Dueppenbecker, Peter, Kiessling, Fabian and Schulz, Volkmar. Software-based Real-Time Acquisition and Processing of PET Detector Raw Data. In: *Biomedical Engineering, IEEE Transactions on* (2015). doi : 10.1109/TBME.2015.2456640.

9. Mackewn, J., Lerche, C.W., Weissler, B., Sunassee, K., Rosales, R.T.M. de, Phinikaridou, A., Salomon, A., Ayres R. ; Tsoumpas, C., Soultanidis, G.M., Gebhardt, P., Schaeter, T., Marsden, P.K. and Schulz, V. PET Performance Evaluation of a Pre-Clinical SiPM-Based MR-Compatible PET Scanner. In: *Nuclear Science, IEEE Transactions on* 62.3 (June 2015), pp. 784790. doi : 10.1109/TNS.2015.2392560.

10. Schug, D., Wehner, J., Dueppenbecker, P.M., Weissler, B., Gebhardt, P., Goldschmidt, B., Solf, T., Kiessling, F. and Schulz, V. ToF Performance Evaluation of PET Modules With Digital Silicon Photomultiplier Technology During MR Operation. In: *Nuclear Science, IEEE Transactions on* 62.3 (2015), pp. 658663. issn : 0018-9499. doi : 10.1109/TNS.2015.2396295.

11. Schug, David, Lerche, Christoph, Weissler, Bjoern, Gebhardt, Pierre, Goldschmidt, Benjamin, Wehner, Jakob, Dueppenbecker, Peter Michael, Salomon, Andre, Hallen, Patrick, Kiessling, Fabian et al. Initial PET performance evaluation of a preclinical insert for PET/MRI with digital SiPM technology. In: *Physics in Medicine and Biology* 61.7 (2016), p. 2851. doi : 10.1088/0031-9155/61/7/2851.

12. Schug, David, Wehner, Jakob, Goldschmidt, Benjamin, Lerche, Christoph, Dueppenbecker, Peter Michael, Hallen, Patrick, Weissler, Bjoern, Gebhardt, Pierre, Kiessling, Fabian and Schulz, Volkmar. Data processing for a high resolution preclinical PET detector based on philips DPC digital SiPMs. In: *IEEE Transactions on Nuclear Science* 62.3 (2015), pp. 669 678. doi : 10.1109/TNS.2015.2420578.

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ling, Fabian and Schulz, Volkmar. PET performance and MRI compatibility evaluation of a digital, ToF-capable PET/MRI insert equipped with clinical scintillators. In: *Physics in Medicine and Biology* 60.18 (2015), p. 7045. doi : 10.1088/0031-9155/60/18/7045.

14. Dueppenbecker, Peter M, Weissler, Bjoern, Gebhardt, Pierre, Schug, David, Wehner, Jakob, Marsden, Paul K and Schulz, Volkmar. Development of an MRI-compatible digital SiPM detector stack for simultaneous PET/MRI. In: *Biomedical Physics & Engineering Express* 2.1 (2016). doi : 10.1088/2057-1976/2/1/015010.

15. Lerche, Christoph W, Mackewn, Jane, Goldschmidt, Benjamin, Salomon, Andre, Gebbhardt, Pierre, Weissler, Bjoern, Ayres, Richard, Marsden, Paul and Schulz, Volkmar. Calibration and stability of a SiPM-based simultaneous PET/MR insert. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 702 (2013), pp. 5053. doi : 10.1016/j.nima. 2012.08.041.

1.7.2 My contributions to the peer-reviewed journal papers

Regarding the first one of the above-listed publications, the idea of quickly interrupting the PET sensors to reduce the PET-based RF interference reduction during MRI RF signal acquisition phase was developed by myself. My ideas to reduce PET-related RF interferences coupled into the MRI RF receive chain by performing FPGA-based clock phase and frequency shifting were published in the second one of the above-listed journal papers. The FPGA firmware improvements needed in order to demonstrate the three different interference reduction techniques via MRI measurement results were done by me and the MRI measurments were performed together with Jakob Wehner. Moreover, I wrote both publications. The works presented in the remaining journal papers (no. three to fifteen) are all based on the Hyperion PET insert plattforms: Hyperion I in case of publications no. 5, 9 and 15, and Hyperion II$^{\text{II}}$ in case of publications no. 3-4, 6-8, and 10-14. The design, imeplementation and characterisation of these PET inserts as a whole were the result of a team effort. My main contributions were

the architectural concepts of the FPGA-based PET data acquisition and control system, the system-wide architecture topology concepts and the communication protocol, as well as the firmware design and major parts of its implementation. I assisted and helped in many of the PET and MRI measurements performed to obtain the results presented in these publications.

1.7.3 Conference records and abstracts

1. Gebhardt, P., Weissler, B., Zinke, M., Kiessling, F., Marsden, P. K. and Schulz, V. FPGA-based Singles and Coincidences Processing Pipeline for integrated digital PET/MR detectors. In: *IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings*. IEEE. 2012, pp. 24792482. doi : 10.1109/NSSMIC.2012.6551565.

2. Gebhardt, P.; Wehner, J.; Weissler, B.; Kiessling, F.; Marsden, P. and Schulz, V. RF interference reduction for simultaneous digital PET/MR using an FPGA-based, optimized spatial and temporal clocking distribution. In: *Nuclear Science Symposium and Medical Imaging Conference Proceedings*. IEEE. 2013, 1-5. doi : 10.1109/NSSMIC.2013.6829138.

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10. Weissler, B., Dueppenbecker, P. M., Gebhardt, P., Salomon, A., Goldschmidt, B., Renz, W., Katharina, S., Zwaans, B., Marsden, P. K., Kiessling, F. and Schulz, V. Design Concept of Worlds First Preclinical PET/MR Insert with Fully Digital Silicon Photomultiplier Technology. In: *IEEE NSS-MIC Conference Proceedings*. M02-3. 2012. doi : 10.1109/NSSMIC.2012.6551484.

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16. Hallen, Patrick, Schug, David, Wehner, Jakob, Weissler, Bjorn, Gebhardt, Pierre, Goldschmidt, Benjamin, Salomon, Andre, Duppenbecker, Peter, Kiessling, Fabian and Schultz, Volkmar. Evaluation of PET performance

and MR compatibility of a preclinical PET/MR insert with digital silicon photomultiplier technology. In: *EJNMMI Physics* 2.Suppl 1 (2015), A55.

1.7.4 My contributions to the conference records and abstracts

In the first one of the above-listed conference proceeding, I proposed the basic principles of the FPGA-based processing pipeline used for both generations of the Hyperion PET inserts and performed the PET measurements to obtain the presented results. In the second conference proceeding, I presented for the first time my ideas on clock frequency and phase shifting applied to DPC sensors of Hyperion PET modules to reduce PET-related RF interferences, which was later published in a peer-reviewed journal paper. The third publication in the list in form of an abstract summarises the RF interfererence reduction technique called RESCUE which was developed by me. I also wrote the manuscripts for the aforementioned conference proceedings and the abstract. Similar to the peer-reviewed journal papers listed in section 1.7.1, I am co-author of, my contributions to the conference proceedings and abstracts no. 4-16 were the design of the FPGA-based PET data acquisition and control system and parts of its implementation for the Hyperion PET inserts. I also assisted in numerous PET and MRI measurements performed for the above publications.

Chapter 2

Background and basic principles

2.1 Positron Emission Tomography

2.1.1 Basic principles

During the mid 1970s, the first positron emission tomography (PET) system with a circular detector arrangement was presented by Ter-Pogossian, Phelps and Hoffman et al. [17], followed by their publications about the underlying basic PET principles [18, 19, 20]. PET, being a nuclear medicine imaging modality, generates functional images from a subject *in vivo* and non-invasively. In this context, a subject may be either a human (clinical imaging) or an animal (pre-clinical imaging). To obtain PET images, various steps are required prior to the actual imaging procedure. First, a pharmaceutical compound needs to be chosen which targets metabolic processes of interest. This compound is then produced and labelled with a radionuclide which emits positrons (β^+). Afterwards, the radio-labelled compound (referred to as a *radio-tracer*) is administered to the patient. Before the imaging process takes place, the patient usually undergoes a waiting period known as the radio-tracer *uptake time* during which the radio-tracer distributes in the body and concentrates at targets of interest. When the uptake time is reached, PET image acquisition procedure is performed. When the area or region of the body of a patient is imaged once, then the actual imaging procedure is known as a static PET scan. When the change in radio-tracer distribution as a function of time is of interest, PET scans of a same region are performed continuously over a period of from several minutes to several hours.

This is known as dynamic PET.

The positron-emitting isotopes used for PET consist of a proton-rich nucleus and achieve stability through decay by converting a proton to a neutron. When a proton is converted to a neutron, a positron and an electron neutrino are emitted [21]. The energy of the emitted positrons is isotope-specific and varies for isotopes used in PET typically between 0.63 MeV for ^{18}F and 3.4 MeV for ^{82}Rb. After its emission, a positron loses its kinetic energy through interactions with the surrounding matter. The average distance travelled by a positron until it comes to near rest depends on the initial energy at emission time and the density and composition of the surrounding tissue. For instance, the average position range of ^{18}F in water is 0.6 mm and the maximum range is 2.4 mm.

When the positron reaches a near-to-rest state, it combines with an electron from a close atom and their masses are converted to electromagnetic energy in the form of two photons that are emitted in opposite directions ($\sim 180°$) as shown in fig. 2.1.

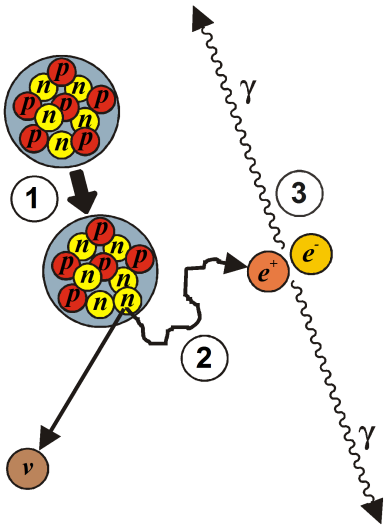


Figure 2.1: Emission of a positron during a proton-to-neutron conversion of a nucleus leading to an annihilation and the release of a neutrino. After having come close to rest, the positron combines with a nearby electron to create two photons with an energy corresponding to the rest-mass energy of the electron and the positron. Both photons are emitted in opposite directions.

This process is known as annihilation [22, 23]. The energy of the two photons

Table 2.1: Overview of radio-isotopes used for PET imaging [23, 24].

Radio-isotope	$t_{\frac{1}{2}}$	$\frac{E_{max}}{MeV}$	$\frac{\text{max } \beta^+\text{range in water}}{mm}$	$\frac{\text{mean } \beta^+\text{range in water}}{mm}$
^{11}C	20.4 min	0.96	5.1	4.1
^{13}N	9.96 min	1.20	5.1	1.5
^{15}O	2.03 min	1.73	7.3	2.5
^{18}F	109.8 min	0.63	2.4	0.6
^{64}Cu	12.7 h	0.65	2.9	0.6
^{68}Ga	68.3 min	1.9	8.2	2.9
^{82}Rb	1.27 min	3.4	14.1	5.9

equals the mass of the electron and positron at rest which corresponds to 511 keV. As a positron may not have dissipated its entire kinetic energy before annihilating with an electron, the remaining residual momentum is conserved by emitting the resulting two photons in a little less than 180 ° from each other, resulting in an acollinearity between them. The angular deviation is gaussian-distributed with a value of 0.5 ° full width half maximum (FWHM).
The rate at which a radioactive sample containing isotopes decays is specified by the *half-life* $t_{\frac{1}{2}}$ and is unique for every type of isotope. As an example, PET isotopes with very short half-lives are in the range of one to two minutes for ^{82}Rb and ^{15}O, respectively, whereas the isotope ^{64}Cu has a half-life of 12.7 hours. An overview of radio-isotopes used in PET imaging is given in table 2.1.

PET imaging is based on the property of the annihilation photons of propagating in opposite directions. By detecting the two photons with detectors located opposite to each other, the line is defined along which the annihilation event happened. This line is known as the *line of response* (LOR). Two photons detected within a specified time window by opposite detectors are said to be in *coincidence*, as they are considered to originate from the same annihilation. Each of the photons detected by a PET detector is referred to as a single event, or short: a *Single*. Analogous to this terminology, two detected singles are said to originate from a coincident event, or short: a *coincidence*. As, due to the random nature

of radioactive decay, singles and coincidences occur at random time intervals, the rate at which they are detected is characterised in *counts per second* (cps).
The most commonly found geometrical detector configuration used for PET scanners is an arrangement of one or more rings with the patient surrounded by the detectors as shown in fig. 2.2.

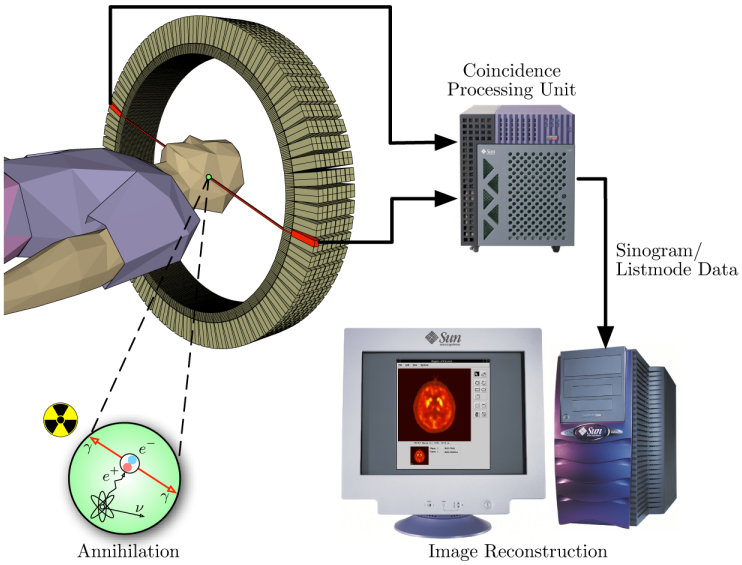


Figure 2.2: A typical PET detector ring configuration used to detect the annihilation photons. Figure reprinted from [25] .

The inner volume surrounded by the PET detectors is known as the *field of view* (FOV). The symmetrical detector arrangement allows the simultaneous capturing of coincident photons over multiple rings which corresponds to three-dimensional (3D) detection of coincidences. In order to detect annihilation photons, commercial and the vast majority of research PET systems use *scintillation* detectors which consist of scintillation crystal arrays which are optically coupled to photo detectors. When annihilation photons interact with the scintillation material, their energy is absorbed and re-emitted as lower-energy-photons with wavelengths in the range of visible to ultra-violet light. These scintillation photons are then converted into an electrical voltage signal with its amplitude being proportional to the energy of the scintillation photons detected by the photo detector. From this, the energy, interaction location and time are determined which represent the information for each single event. A coincidence processor (see fig. 2.2) subsequently determines pairs of coincident singles as those located

within a FOV acceptance angle and detected within a small time window, known as the *coincidence timing window*, of each other. The latter usually lies in the range of a fraction of a nanosecond to several nanoseconds. It accounts for the photon travel time from any annihilation location along all possible LORs within the FOV and additionally depends on the detector technology and related differences in signal propagation delays within a PET system.
The number of coincidences detected by a detector pair during a measurement is proportional to the total amount of radioactivity along the LOR between that detector pair (i.e. the line integral along that path). Using spherical coordinates, all line integrals through the radioactivity distribution at a given angle are called a *projection*. The projection data for many different angles is usually histogrammed in a set of two-dimensional (2D) matrices known as sinograms [26]. As an alternative to sinogram data, some PET systems store and output the measured coincidences data in a *list-mode* file which contains information about the detector coordinates of the LOR position for each detected Coincidence. Depending on the PET system, the LOR information may be accompanied by energy and time-stamp values as well as the time difference between the two single-event detections. Afterwards, either a list-mode file or the sinogram data are transferred to an image reconstruction algorithm to obtain original the radioisotope distribution from the projections. To reconstruct PET images, analytic algorithms such as *filtered back projection* (FBP) or iterative ones such as *maximum likelihood - expectation maximisation* (ML-EM) [27] or the computationally accelerated version called *ordered subset - expectation maximisation* (OS-EM) [28] are commonly used. An advantage of analytic reconstruction algorithms is their fast-computation-related properties. However, they suffer from poor noise-related properties due to the difficulty of modelling accurate Poisson-statistics of the measurement data. This issue is addressed by the iterative reconstruction algorithms which can incorporate a detailed model of the acquisition process, including the statistical nature of the acquired data, and yield improved image quality [23]. A disadvantage compared to analytical reconstruction is, however, that they are computationally demanding. While these were not practicable during the Nineties due to the lack of performance as offered by computers, iterative reconstruction has been taking a more and more important role for PET image reconstruction thanks to the ongoing increase in computation performance.

2.1.1.1 Limitations of PET

The spatial resolution in PET describes how precisely nuclear decay events can be localised within the PET field of view. It is limited by several factors which are described in the following.
The positron range and the effects of the acollinearity both define the fundamental lower limit of the spatial resolution in PET. A larger positron range increases the distance between a detected annihilation and the actual location of interest which is the $\beta+$ emitter. The larger mean range leads to decrease in resolution due to a larger blurring effect [26]. For the isotopes listed in table 2.1, the mean range in water varies between 0.6 mm and 5.9 mm
The acollinearity between two annihilation photons introduced because of the positrons' conservation of momentum also leads to a resolution decrease [29] which is given approx. by $tan(\pm 0.25\,^{\circ}) \times 0.5d$ with d being the inner diameter of the PET detector ring [26] and $\pm 0.25\,^{\circ}$ being the angular uncertainty (see fig. 2.3).

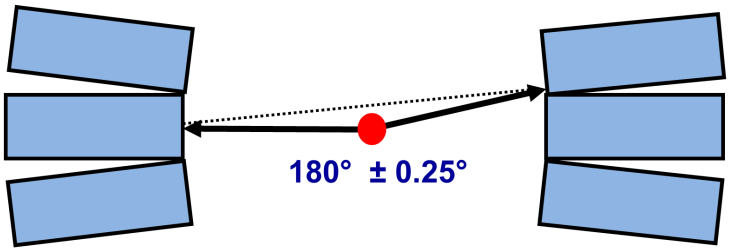


Figure 2.3: The acollinearity effect defines a lower limit of the spatial resolution. The effect is drawn disproportionately to visualise the effect.

For a clinical PET system with a diameter of 90 cm , the decrease in resolution related to the effects of acollinear photon emission is 1.96 mm while for a preclinical PET detector ring with $d = 20$ cm, the resolution is reduced by 0.44 mm.
The tangential and axial dimensions of a scintillation crystal (being an element of a scintillation crystal array) facing the centre of the PET FOV determine the intrinsic spatial resolution of a PET detector. The resolution equals half the crystal width for a β^{+}-emitter source located at the mid-point between the two opposite crystals. The resolution linearly decreases towards the value of the crystal width

as the source moves towards one of the crystals. [22]. This yields a non-uniform spatial resolution across the FOV.
Depending on where in the FOV the annihilation photons are emitted, their geometric detection location can negatively affect the spatial resolution due to a phenomenon known as the *parallax* effect [23]. An annihilation located at the centre of the FOV is detected and correctly located by two opposing detectors regardless of the interaction depth of the annihilation photons within the scintillation detector. However, as shown in fig. 2.4, the further the annihilation source is distant from the centre of the FOV, the higher the likelihood becomes that the detected LOR is mispositioned. This happens as the annihilation photons enter the crystals not perpendicularly to the crystal face any more, leading to an uncertainty related to the LOR positioning.
The first two factors create limitations in spatial resolution due to physics related to positron emission and annihilation, whereas the last two factors limit the resolution due to the PET-detector-related properties and the scanner geometry.

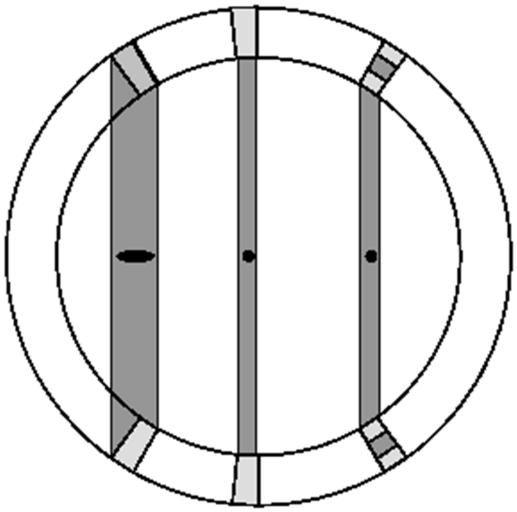


Figure 2.4: Visualisation of the parallax effect: An annihilation event occurring close to the iso-centre enters the scintillation area facing the cenre of the FOV almost tangentially, resulting in a lightly degraded positioning. However, the photons of an event occurring far from the centre of the FOV (left example) cross the scintillation area at an oblique angle. The photon detection occurring in neighbouring detectors leads to large LOR positioning uncertainties.

The sensitivity S of a PET system describes how many coincidences are detected per time unit in comparison to the radioactivity present in the PET system's FOV. It is influenced by the geometric and intrinsic efficiencies, the defined photon energy window (introduced in section 2.1.2.1), PET system dead time and absorption and scatter of the radiation between its source and the PET detectors. The geometric efficiency results from the solid angle covered by the total PET detector surface at distance r from the radioactive source. The intrinsic efficiency describes the ratio of annihilation photons penetrating the scintillation material and those interacting with the material to produce scintillation light detectable by the photo detectors. The sensitivity for a point source in the centre of the FOV can be calculated by

$$S = \frac{A\epsilon^2\gamma}{4\pi r^2} \frac{coincidences\ per\ second}{MBq} \tag{2.1}$$

with r being the PET FOV transaxial radius, A the scintillaton material area, ϵ the intrinsic efficiency, and γ the attenuation factor [30].

At a given sensitivity during a PET data acquisition procedure, all coincidences detected by a PET system are denoted as prompt coincidences or for short *prompts*. However, not all of them contribute to the desired signal in terms of obtained LORs mapping actual annihilation points. One reason for this is the interaction of photons with any other kind of matter. Due to a physical effect known as *Compton scattering* which is the dominant type of scatter for photons with energies in the range between 100 keV and 10 MeV in the case of body tissue [26]. When a Compton interaction occurs between an annihilation photon and an electron, the photon transfers a part of its energy to the electron and gets scattered in another direction. Thus, photons may interact with tissue or bone matter before they enter the scintillation detector which leads to a falsely assigned LOR between the detectors as shown in fig. 2.5("Scatter"). Compton scattering also occurs in scintillation detector material. Another undesired effect describes the detection of two annihilation photons which do not originate from a same annihilation (see fig. 2.5("Random")). This can happen when two singles are detected within the coincidence timing window of the PET scanner. Coincidences are then assigned by mistake from annihilation events which never took

place along the determined LOR which are known as *randoms*. The randoms rate is proportional to $2\tau s^2$ with τ being the coincidence timing window and s being the singles rate [23]. This means that the randoms rate increases quadratically with the singles rate and thus with the activity concentration. A third effect occurring during a PET measurement are multiple coincidences or short *multiples*. When more than two annihilation photons are detected within the coincidence timing window, then a unique LOR cannot be determined and the singles are discarded (see fig. 2.5("Multiple")). The fraction of scatter and randoms are usually estimated during data processing. Subtracting these from the prompts yields the true coincidences or in short *trues* (shown in fig. 2.5("True")) which are used for image reconstruction.

Scattered coincidences solely result from underlying physical properties i.e. interaction between photons and electrons. The scatter fraction (compared to all acquired coincidences) can be reduced by narrowing the energy range. The latter is used as a criterion to reject detected scattered annihilation photons as their energy is below the defined energy range from photons with energies close to or of 511 keV. This is presented in more detail in section 2.1.2.1. The detection rate of randoms and multiples result from PET system properties. Both can be reduced by narrowing the coincidence timing window. Detected multiples are discarded and therefore do not impair the PET image quality. Scatter and randoms coincidences, however, cannot entirely be detected, corrected or removed and thus affect the image quality. As the randoms rate is singles-dependent, a radio-tracer activity outside of the PET FOV increases the randoms rate due to singles from outside of the FOV entering the scintillation detectors. For instance, a clinical PET scan with FDG as a used tracer, the randoms rate may be greater than 50 % of the prompt rate [31].

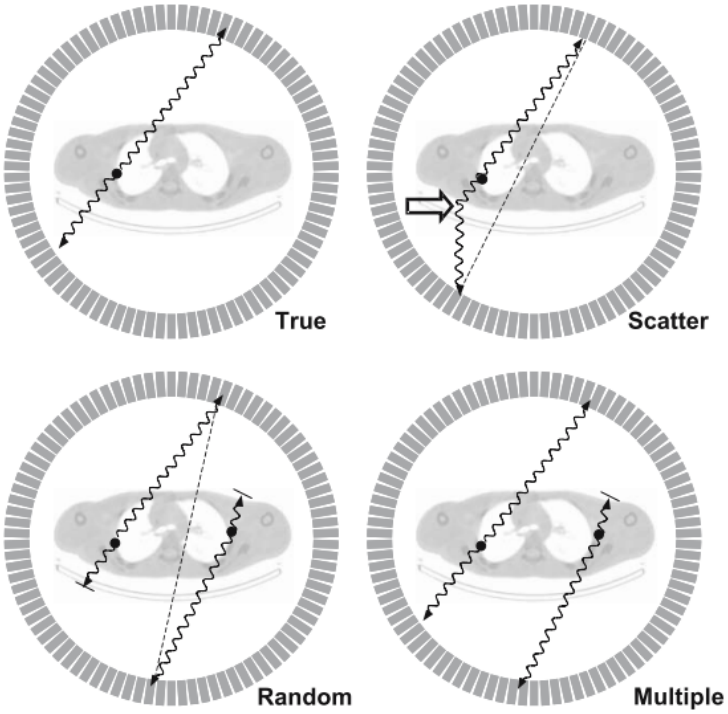


Figure 2.5: Different types of coincidences occurring during a PET measurement: a true coincidence, a scattered coincidence introduced by interaction with matter, a random coincidence falsely determined from two unrelated annihilation photons, and a multiple coincidence. The latter is a result of three or more detected singles within the coincidence timing window that are immediately discarded by the coincidence processor. Figure reprinted with permission from [23].

Generally, a measured signal value contains the desired, wanted information or *signal* which is superimposed with an error or *noise* which is unwanted. The type of error can be a systematic one, meaning that it superimposes repeatedly with all measured signal values by a consistent value. Another type of error is the randomly occurring one (known as *statistical* errors) which either happens because of randomly occurring quantities to be measured or because of physical limitations of the measurement tools. The quality of a measured signal can be characterised by means of the amplitude of the desired signal compared to the unwanted noise and is given by the *signal-to-noise ratio* (SNR). PET data originates from randomly occurring radio-isotope decays and is thus statistically variable [26]. Therefore, a PET measurement represents an average of independent data points over the acquisition time and the limited amount of detected data results

in uncertainties which are considered as *noise*. Given the Poisson-distributed decay process which is measured as an average amount of coincidences over time, the noise equals the square root of the number of measured coincidences [32]. This means that measurements with a smaller number of coincidences will result in data with a higher noise fraction compared to data sets with a large number of coincidences, as the square root of N measured coincidences grows slower than the coincidences amount as such. Typically, a clinical PET data set should contain at least 10^6 coincidences in order to reconstruct a meaningful image [22]. The number of measured coincidences mainly depends on the measurement time, the radio-isotope dose and the PET scanner configuration. But neither the measurement time, nor the dose can be increased arbitrarily for a PET scan. In fact, the administered radioactivity dose is kept as low as possible to expose the patient to as little radiation as possible. The measurement time is usually a trade-off. On one hand, it should be short enough satisfy the patient-comfort and ease the daily clinical practise flow and on the other hand it should be long enough to collect sufficient data to obtain satisfactory PET images. Therefore, the PET detector technology and the image reconstruction algorithms used for PET (as well as SPECT) have been continuously improved to increase image quality for constant scan times and injected radio-tracer dose.
In addition to the statistical noise related to the random nature of nuclear decay, effects such as scattered and random coincidences introduced by limitations of the PET system add statistical noise to the measurements which, in turn, negatively affect the SNR of PET images. For a measurement at a given prompt rate, the noise added by randoms and scattered coincidences can be characterised by the *noise-equivalent count rate* (NECR) [33] which is defined as

$$\text{NECR} = \frac{T^2}{T + S + \alpha R} \tag{2.2}$$

with T, S and R being the true, scattered and random coincidence rates, respectively. α varies between one and two depending on the type of random correction technique applied. The NECR describes a coincidence rate which is equivalent to a measurement without scatter and randoms in terms of SNR in the data. It is measured according to a measurement procedure with an imaging phantom of defined size and uniform activity concentration as specified by the

National Electrical Manufacturers Association (NEMA) [34]. The NECR serves as a measure to determine the impact of a given prompt coincidence rate on the image quality and is according to [26] roughly proportional to the square of the SNR determined for the PET image activity values in a phantom measurement. The NECR is dependent on the size and activity distribution of the scanned object, as the NECR takes into account the scattered coincidence rate.

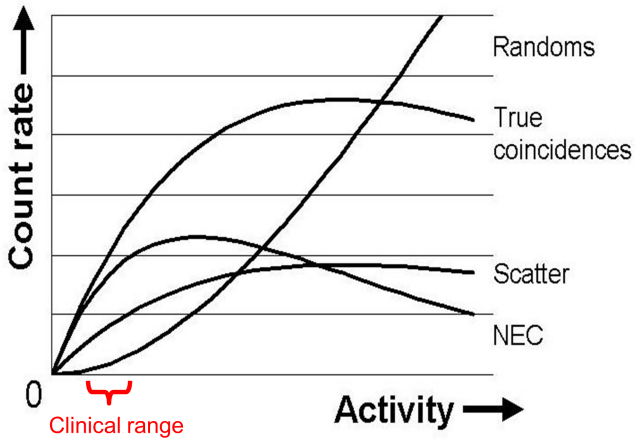


Figure 2.6: The rates of different types of coincidences over an activity range typically measured for a clinical PET scanner: With increasing activity, the true coincidence rate decreases due to to an increasing dead-time. As the noise-equivalent count rate (NEC) takes into account the randoms and scattered coincidences, it will always be lower than the trues rate.

Another type of statistical noise is added by electronic circuits and the underlying type of technology used. As examples, photo detectors as well as electronic signal amplifiers tend to generate noise in form of small voltage fluctuations which add to and so degrade the signal information of interest. Analogue amplifiers do amplify the signal shape at their inputs, meaning that unwanted noise is amplified together with the actual signal of interest. A further example is long cabling that is prone to pick-up of statistical noise particularly when being exposed to external electromagnetic fields. Any electrical noise added in the PET signal path that influences the electric signal shape so that noise cannot be retrospectively filtered from the original PET signal might impair the resulting PET images negatively. It is therefore crucial to design a PET system with low-noise-generating electronics to keep the electronic PET SNR and thus the image SNR unaffected.

2.1.2 PET detector technology

2.1.2.1 Scintillators

Scintillation materials are nowadays commonly used for gamma-ray (i.e. the annihilation photons) detection in PET and are therefore an integral part of PET detectors. Scintillators usually consist of an inorganic crystal structure which emits light with a particular spectrum in the visible to ultraviolet light range as a consequence of annihilation photon interaction with the crystal structure. The emitted light is then detected by photo detectors which are usually optically coupled to the scintillator. Due to their material structure, PET scintillators are also called *crystals*. The energy converted to scintillation light after the interaction of annihilation photons with scintillation matter is measured via the light intensity. The latter is converted in an electronic pulse height by the photo detectors and the height distribution is known as the *energy spectrum*. Figure 2.7 shows two energy spectra typically obtained for ^{18}F and ^{22}Na with a PET detector. Annihilation photons with energy ranges as used for PET mainly interact with the crystal material via Compton interaction [23] by partially depositing their energies during each electron interaction with the latter introducing the scintillation light generation process. Scattered annihilation photons may Compton-interact with matter repeatedly until their energy is absorbed or leave the scintillation crystal after scattering with a lower energy. In the case of Compton interaction, the measured deposited energy covers a continuous range of the energy spectrum obtained for annihilation photon interaction with PET scintillators which is known as the *Compton range* [26]. In the case of a photoelectric absorption, all energy of the gamma-ray is deposited and the measured pulse height of ideally 511 keV is called a *photo-peak*. Multiple scatter interactions followed by an absorption also lead to a photo-peak, as the complete annihilation photon energy is eventually deposited in the crystal. The peak is denoted in FWHM and well distinguishable from the rest of the spectrum as seen in fig. 2.7(a) and fig. 2.7(b). Next to the photo detector properties and the PET detector geometry, scintillator properties required for PET to extract the desired information from annihilation photon interactions have a predominant influence on the PET scanner performance. The properties of main interest are the energy resolution, annihilation photon stopping power, scintillation light decay time and the light output.

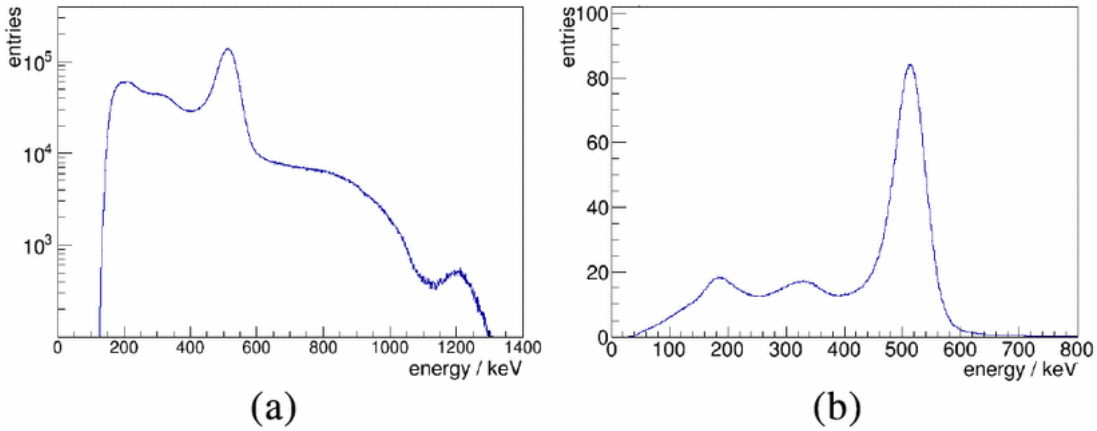


Figure 2.7: Energy spectra measured with a PET detector: Figure (a) shows a spectrum obtained with ^{22}Na, figure (b) was measured using ^{18}F for a relative amount of annihilation photons. In both figures, the Compton energy range between approx. 250 keV and 400 keV and the photo peak around 511 KeV are visible. Additionally, figure (a) reveals an additional peak at 1275 keV which is only obtained with ^{22}Na. (© 2015 IEEE. Reprinted, with permission, from [35]).

These properties partially conflict with each other. A high stopping power increases the probability to detect annihilation photons and is obtained by a high atomic number and material density as it decreases the attenuation length. The light decay time should be as low as possible to allow for a differentiation between two successively detected annihilation photons within short time windows (i.e. at high coincidence rates). A second photon interacting in a crystal while the scintillation light of the previous detection has not fully decayed may lead to pulse *pile-up*. Here, the total energy detected by the photo detector(s) may exceed the photo peak, normally leading to a rejection of the detected interactions by the detector electronics as the total energy cannot be separated and assigned to the different annihilations photons. A short decay time also allows to narrow the coincidence time window in order to reduce the randoms rate. The higher the light output, the better the energy resolution of a scintillator. A good energy resolution helps to distinguish Compton-scattered interactions from interactions leading to a photo-peak and consequently reject scattered coincidences to increase image SNR and thus the quality.
Increasing the crystal length in radial direction of the PET FOV increases the intrinsic efficiency which, in turn, leads to a sensitivity increase of the PET sys-

tem. On the other hand, the interaction localisation accuracy becomes worse due to increased depth-of-interaction issues (parallax error), resulting in a lower spatial resolution towards the transaxial edges of the FOV. Moreover, longer crystals also lead to a higher scintillation light propagation time, meaning that the timing resolution is decreased. This impairs the time-of-flight performance for clinical PET systems with TOF capabilities.
The scintillation light is converted to electrical pulses by photo-detectors. The different photo-detector technologies used in PET are discussed in the following sections.

2.1.2.2 Photo-multipliers

A photo-multiplier tube (PMT) is device that can detect very weak light intensities to convert these into large electrical signal pulses. The electrical signal is proportional to the number of photons detected. A PMT consists of an evacuated chamber made of glass which contains a photo-cathode, dynodes and an anode. The photo-cathode is located at one end face of the PMT and is coupled to the scintillator. Scintillations photons generated by the scintillator interact with the photo-cathode material by releasing electrons via the photo-effect. A high optical-to-electrical conversion efficiency is desirable, and this is a function of the scintillation light wavelength. A large potential difference (typically in the order of kV) is applied across the photo-cathode, the cascaded dynodes and the anode. Electrons released from the PMT photo-cathode are accelerated and then hit the first dynode among the cascade of dynodes to release further electrons. The electrons released at the first dynode are then accelerated towards the second dynode again releasing further electrons as a consequence of interactions with the dynode material. After striking the last dynode, the electrons reach the anode. At the anode, a large electrical signal pulse (typically amplified by 5-7 orders of magnitude) can be measured at the PMT output pins.
PMTs have been used since the early days of PET. These devices are well understood and technically mature. The signal amplification of the signal is in the order of 10^5 to 10^7 and is essentially noiseless allowing read-out of the very low light intensities provided by the scintillators [26]. The efficiency of a PMT in releasing an electron from the photo-cathode as a result of a scintillation photon

absorption is known as the *quantum efficiency* (QE) and is typically in the range of 25 % (i.e. 1 in 4 photons release an electron) [23]. More recent PMT developments, however, have led to an increase in QE to around 40% in some situations [36].
The acceleration of electrons in the direction of the dynodes and the anode is fundamental for the PMTs to work properly. Operation within a magnetic field is therefore impaired due to the Lorentzian force which leads to a deflection of electrons during their movement. Consequently, PMTs are not suitable for operation within strong magnetic fields as used for Magnetic Resonance Imaging. The dimensions of PMTs typically used for medical imaging are in the range of single-digit centimetres and are therefore not suitable for PET systems with design requirements related to highly compact detectors (although multi-anode and position-sensitive PMTs have found use in some applications).

2.1.2.3 Avalanche Photo-Diodes and Silicon Photo-multipliers

Another device suitable for scintillation-light detection and proportional conversion to an electrical signal is hte photo-diode. Photo-diodes are semiconductor-based with foot-prints and a thickness in the range of millimetres and are therefore very compact compared to PMTs. An avalanche photo-diode (APD) is operated with a reversely biased voltage and is from a functional point-of-view divided into a light absorption region and a gain region. When scintillation light interacts with the lattice of the absorption region, an electron-hole pair is generated and the electric field across the absorption volume accelerates the pairs. When the energy provided by the electric field is sufficiently high, then the drifting electron-hole pairs are able to release further electron-hole pairs during collisions with the material structure (ionisation process). The gain region of the APD is therefore characterised by a very high electric field which allows for a chain reaction of pair generation known as the avalanche effect.
Typically, APDs offer a gain of 10^2 to 10^3 which is at least three orders of magnitude lower than that of PMTs. However, the quantum efficiencies are generally much higher than those of PMTs (up to 80%). As the electron acceleration in these devices occurs only over extremely short distances, effects observed for PMTs during operation in magnetic fields are very small. APDs are not suitable

for TOF PET due to their slow signal response time which is in the nanosecond range. Besides the low APD gain, the gain stability is highly dependent on the bias voltage and the temperature. This requires sophisticated voltage regulation and temperature control to provide for a stable operation, e.g. within a PET system, without gain drifts during PET image acquisition.

When an APD is operated with a further increased reverse-biased voltage, the device enters an operating region called *Geiger-mode*. At high voltages, a single photon absorption may introduce a Geiger-discharge, leading to a large output signal that is not proportional to the light photon intensity any more. Instead, it shows a binary behaviour. However, by grouping a large number of very small Geiger-mode APDs (also known as *single-photon avalanche diodes* (SPAD)) with sizes ranging between 20 μm and 100 μm into an array of cells, a signal output proportional to the light intensity can be obtained. Such arrays of very small SPADs, or cells, are also known as silicon photo-multipliers (SiPM). SiPMs have gains similar to those of PMTs and have an improved SNR compared to APDs. The Geiger-discharge-related signal response is fast, allowing time resolutions and ranges of one hundred picoseconds [37]. Therefore, SiPMs are suitable for TOF PET.

Normally, only a fraction of the SiPM device area is sensitive to scintillation photons, i.e. the surface covered by the actual cell array. The quantum efficiency, however, only applies to that photon-sensitive area. Thus, the *photon detection efficiency* (PDE) is considered which not only takes into account the quantum efficiency, but also the fraction of the photo-detector that is light-sensitive. The PDE of SiPMs lies in the range of 30 % to 40 % [38]. Due to the nature of semiconductors, SiPM cell avalanche may not only occur as a consequence of an absorbed photon, but may also happen as a result of thermal excitation of electrons in the lattice. These unwanted avalanches constitute a *dark count rate* that results in statistical signal noise. The number of dark counts per time interval increases with an increasing operating temperature of SiPM cells [39]. The resulting noise can be discriminated, to a little extent, by readout front-end electronics by setting a signal threshold in order to separate dark counts from larger, real scintillation-photon-triggered SiPM signals.

2.1.2.4 Philips Digital Photon Counter

The photo-detectors presented in the sections 2.1.2.2 and 2.1.2.3 all have in common that they output an analogue electrical current as a measure of photon detection. These signals are fed to front-end electronics (the electronic signal processing circuits closest to the photo-detectors) where they usually undergo further amplification by local pre-amplifiers and processing to enable PET singles and coincidence detection. Firstly, temporal information in the form of a time stamp is generated and added as the signal detection time. Secondly, positioning information is determined and added. Thirdly, the signal pulse height is integrated over time to determine the number of scintillation photons and from this the energy deposited during annihilation photon interaction in the scintillator. These tasks were performed in the past by analogue front-end electronic circuits but these are now increasingly being replaced by mixed-signal *application-specific integrated circuits* (ASIC). Generally, ASICs are integrated semiconductor devices designed and produced for particular tasks. The terminology *mixed-signal* indicates that a device operates and deals with analogue as well as digital signal information. Mixed-signal ASICs used in PET front-end electronics usually preprocess analogue photo-detector signals prior to performing an analogue-to-digital signal conversion. As a result, the ASIC outputs digital PET photo detector information in the form of a time-stamp, photo-detector position information and an energy value.

The use of ASICs allows for further steps towards compact PET detector designs by replacing the former front-end electronic designs using multiple components per detector channel with a single chip offering multiple detector channel inputs [40, 41, 42, 43, 44]. A further step in photo-detector evolution towards an increased detector component integration was introduced by Philips in 2009 with the *digital photon counter* (DPC) [45, 46]. The DPC sensor is a chip which consists of a monolithic *silicon die* [47], also referred to as a *sensor die*. It houses an array of SPADs (SiPM cells) as well as digital circuits that determine time stamp, position and energy information following the SiPM signal detection. The sensor die of type "DPC 3200-22" is shown in fig. 2.8(a) and comprises four SiPM pixels in a $2x2$ arrangement. Each pixel consists of 3200 SPADs divided into four sub-pixels with 800 SPADs each. Every sub-pixel has 25 *row trigger lines*, each

consisting of 32 SPADs. SPADs having much higher *dark count rates* (DCR) than the average, e.g. due to chip production tolerances, can be deactivated (inhibited) individually. Every SPAD avalanche is stored as binary information. This information is read for every SPAD of a pixel and summed during a read-out procedure. The latter is only initiated when both a low-threshold trigger and a consecutive high-threshold trigger are reached which are both a result from logic interconnections of SPAD break-down signals and explained in the following.
Four different low-threshold trigger schemes are available and are referred to as schemes 1 to 4, or *first*, *second*,*third* or *fourth photon*. Scheme 1 results in a trigger as soon as a SPAD breaks down (i.e. an avalanche occurs) in one of the four sub pixels of a pixel. The higher trigger scheme settings set a combination of logical AND or OR operations between the sub pixels, resulting in combinations of multiple SPADs required to break down in order to generate a trigger. The trigger logic is shown in fig. 2.8(b). The logic interconnection of the sub-pixels for each trigger scheme setting is listed in table 1 of [48].

Any further course of action followed by a detected low-threshold trigger is controlled by a digital, clocked, *finite state machine* (FSM) in the DPC sensor's main acquisition controller (shown in fig. 2.8(c)). A finite state machine is a logic circuit with a finite amount of states that describe a predefined course of actions which can depend on external events. Depending on the currently active state (i.e. the *current state*), a sequence of events can cause state logic to trigger output signals and/or transition to another state. In the case of the DPC sensor, upon a detected trigger-scheme-dependent lower-threshold trigger, the event-acquisition FSM enters a validation phase of configurable length. During this time, a programmable trigger validation condition needs to be fulfilled to successfully validate the high-threshold trigger using a logic operation network similar to the one shown in fig. 2.8(b). More details on the structure of the high-threshold trigger logic (validation) can be found in [48]. The average number of SPAD break-downs needed to reach that threshold in one pixel depends on the chosen validation condition and is listed in table 2.2.

The event-acquisition FSM enters the *integration* state upon a successfully validated trigger. It serves the purpose to wait and collect for SPAD breakdowns resulting from the scintillation photons for a programmable amount of time. Sub-

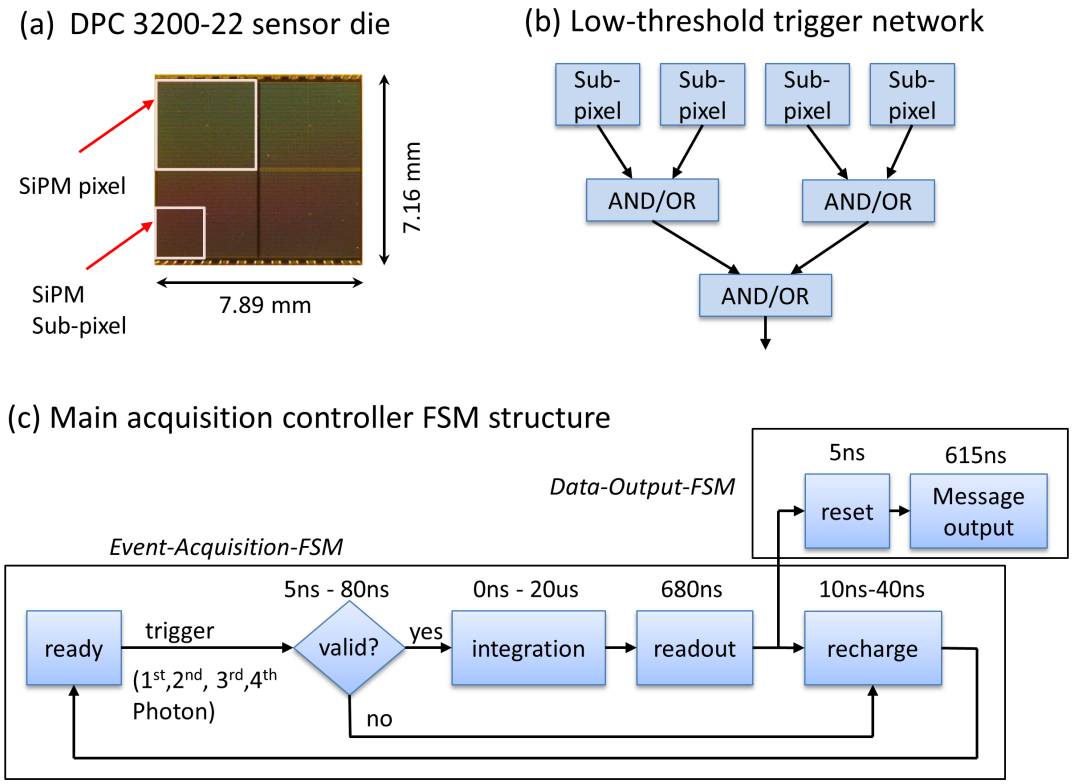


Figure 2.8: Figure (a) visualises a DPC sensor with four pixels seen from the top, (b) depicts a simplified tree-based validation network with logic stages configurable to perform either AND or OR logic for low-threshold trigger, (c) shows the structure of the two finite state machines implemented in the main acquisition controller of a sensor die. Figure (c) was reprinted and adapted from [49].

sequently, the *readout* state is entered, during which the total number of SPAD breakdowns for all the four pixels are summed up. During the *recharge* state, the SPADs are reset so that the sensor die is ready for new triggers.

The DPC sensor is operated with a clock frequency of 200 MHz which is directly fed to a subset of the digital logic such as the FSMs of the main acquisition controller (FSM state diagrams shown in fig. 2.8(c)). Other parts of the digital logic like the time stampers are clocked with half that frequency which is generated by a DPC-sensor-internal clock frequency divider.

The time stamper consists of a coarse counter and a fine counter. The latter consists of two time-to-digital converters with tap delay lines. The delay lines have 512 bins with bin widths between 20 ps and 25 ps in order to provide a high tim-

Table 2.2: Validation network setting range (hexadecimal notation) and resulting minimum and average number SPAD breakdowns needed to successfully validate a trigger [35].

Validation network setting	average SPAD number	min. SPAD number
$0x55$	16.9 ± 6.2	4
$0x54$	27.5 ± 10.3	4
$0x50$	37.1 ± 12.8	6
$0x00$	52.2 ± 15.0	8

ing resolution. A larger time range is covered by the 15-bit-wide coarse counter running with a clock period of 10 ns, thereby covering a time of $2^15 = 327.68\,\mu$s. A time stamp is generated in the DPC sensor whenever the low-threshold trigger is reached. Thus, the higher the trigger scheme number, the larger the time window between the first detected photon and the time stamp generation. A higher trigger scheme helps to decrease the dead-time at high dark count rates, but this occurs at the expense of the timing resolution.

The transition from *readout* to *recharge* initiates the DPC sensor message generation and transmission by triggering the *data-output* FSM as depicted in fig. 2.8(c). A message start bit followed by a 120-bit-wide message is transferred at a clock frequency of 100 MHz in parallel over two data output lines. Each DPC sensor message always contains the number of summed-up SPAD break-downs for all four pixels. This means that a successful trigger by one pixel initiates the readout and data transmission of information from all DPC sensor pixels of a single sensor die. As the total time needed to output a sensor message (620 ns) is always shorter than the minimum time required for the event-acquisition FSM to perform a complete FSM cycle (695 ns), a seamless output of acquired photon-interactions is possible. In addition to data messages, the DPC sensor can be configured to output a *framing message* to report coarse counter overflows. Framing messages differ from data messages by an asserted *overflow*-Bit. A coarse counter overflow occurring while the event-acquisition FSM is processing a trigger leads to latching of the framing packet output, meaning that it is transmitted as soon as the last trigger has been processed. Because the DPC sensor autonomously outputs messages, the message receiver needs to be able to detect and be ready to receive

DPC sensor messages at any time.
The DPC sensor is configured with inhibit-settings for all SPADs as well as the configuration parameters used, e.g. for the trigger scheme, validation network and validation time, via a serial data interface defined by the *Joint Test Action Group* (JTAG) standard. Multiple DPC sensors can be configured at once by connecting their JTAG in- and output lines to form a JTAG-chain which can be clocked at a maximum frequency of 50 MHz.
An external trigger signal can be applied to the sensor die to force an internal successfully validated trigger. This may be useful to collect and read out the number of broken-down SPADs of a DPC sensor while the internal trigger condition was not met. As an example of the use of a forced trigger for PET detectors, the edge of a scintillation light distribution may reach a DPC pixel where only a very small number of photons interact with the SPADs. Although the internal trigger validation was not met, an externally-triggered, forced read-out may add additional information to localise an annihilation photon more accurately by adding this information to data from neighbouring sensor dies.
To distinguish it from SiPMs providing analogue signals, the DPC sensor is said to be a *digital SiPM* (dSiPM).
The behaviour of the DPC sensor FSMs, the amount of data per sensor message, the configuration procedure and the internal and external trigger conditions are all crucial to understand in order to design a data acquisition system which needs to configure, control and read out the DPC sensors. This will be presented in chapter 3 and the demonstration of the MRI RF interference reduction methods presented in chapters 4 to 6 are based on the behaviour of the DPC sensor's digital logic and its control.

2.1.2.5 PET detector design

PET detector rings commonly consist of multiple units, each of which houses the scintillation material with underlying photo-detectors. The scintillator is usually arranged in an array of scintillator elements with a material between them having good reflective properties. This avoids scintillation light from spreading to neighbouring crystals on the way towards the photo detectors in order to preserve spatial and timing resolution. When the crystal size is smaller than the

underlying photo-detector, a light guide is placed between the two in order to spread the scintillation light over more than one photo-detector. The crystal in which the annihilation interaction occurred can then be determined, or *spatially resolved*, by applying a weighted centroid positioning algorithm, also known as the *Centre-of-Gravity* (CoG) or Anger algorithm, or a similar procedure. The position of a crystal in the crystal array is determined by calculating the position-weighted sum of the photo-detector signals and dividing it by the total sum of all detector signals [26]. This approach allows the use of photo-detectors larger than the crystal sizes with the spatial resolution still determined by crystal dimensions. Detector configurations falling into this category are the block detector and quadrant-sharing detector designs [23]. The use of photo-detectors larger than the crystal sizes is driven by two main reasons. Firstly, depending on dimensions of the crystal elements, an appropriate photo-detector of the same size may not be commercially available. Secondly, detectors with smaller sizes result in a larger number for a given total scintillator area. This not only increases the costs related to number of photo-detectors, but also the costs related to front-end electronics and data acquisition system due to the increased number of detector channels to process. Therefore, this approach is typically used by commercially available, clinical PET systems.
Instead of light-sharing, another possibility is to directly couple each crystal element to a dedicated photo-detector, known as *one-to-one* coupling. This approach is usually costly and technically demanding because of the resulting high number of detector channels. However, the lack of light-sharing by an intermediate layer is advantageous for a high spatial resolution and lower system dead-time. Except for clinical PET/CT scanner *Vereos* recently announced by Philips [50], this configuration is so far implemented for research prototypes and pre-clinical PET systems only.

2.1.3 PET data acquisition

In the context of imaging instrumentation in nuclear medicine, the task of data acquisition systems is to collect and process information provided by the photo-detectors through front-end electronics upon annihilitation photon interaction within the scintillators. As introduced in section 2.1.2 for PMTs, or semiconductor-

based APD or SiPM sensors, the information is either provided by analogue signalling or in case of dSiPMs provided in form of digital messages. Important characterisation parameters of an acquisition system are the throughput and the dead-time behaviour, as they have a direct impact on the effective sensitivity of the PET scanner.

Throughput in the context of a digital communication system is defined as the rate of data or data message delivery over a communication channel and measured in *bits* (or *bytes*) *per second*, or measured in *data messages per second*. In the same context, the *bandwidth* of a communication channel corresponds to the throughput and both terms are used synonymously. In a communication system with communication links connected in series, a link with a maximum throughput lower than those of the other links is referred to as the *bottleneck*.

Dead time in the context of an acquisition platform represents the ratio of data which could not be read and/or processed, to data which would have been read and/or processed assuming a linear behaviour [51, 23]. Over an aimed throughput range, the throughput behaviour should remain unchanged and predictable. As an example, an oscillating throughput behaviour introduced by improperly specified or implemented parts of a platform might lead to temporary data loss. The throughput range of an acquisition platform should cover the maximum throughput rates expected for the target PET-system and its target applications. Ideally, the aggregate throughput range of the acquisition system should match the throughput range expected by the photo-detectors at leats up to the point where the PET detector dead time starts to increase. This would result in a balanced dead-time behaviour between the PET detectors (including front-end electronics, if needed) and the underlying acquisition platform.

The rate at which detected annihilation photon interaction events must be read and processed depends on the following parameters:

1. Number of triggered photo-detector channels, or *hits*, per gamma photon
2. Tracer-isotope-type and -activity
3. Scanner geometry
4. Scintillation material and shape
5. Detector-types and -sizes

6. Data amount per hit

When the PET detector design uses light sharing, one or more photo-detector channels may trigger and transmit a signal as a consequence of a gamma photon interaction. The number of triggering channels depends on several factors such as the scintillation material and shape, the light guide material, thickness and shape, the trigger threshold settings, the gamma photon energy and the gamma location of interaction in the scintillator. A triggered photo-detector channel is also referred to as a *hit*. Using this nomenclature, a single gamma interaction leads to the generation of several hits when light sharing is used, as visualised in figure fig. 2.9. The average number of hits per single event has a large influ-

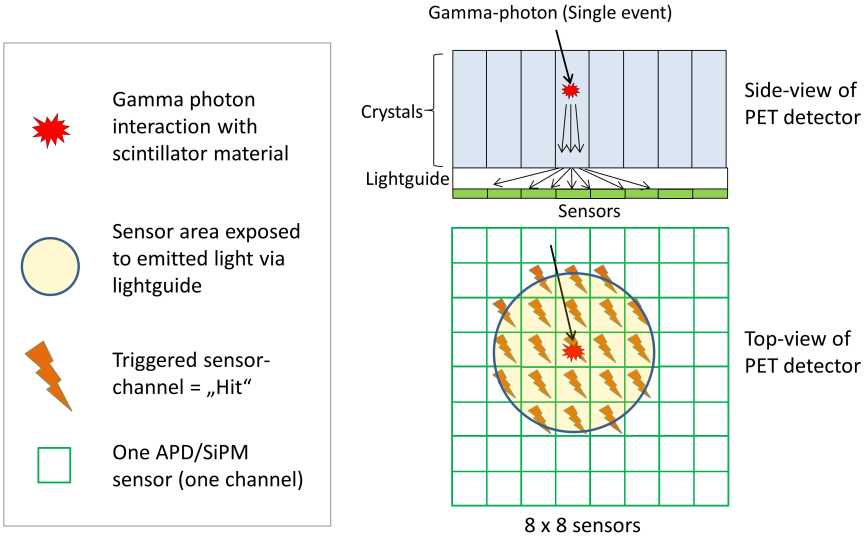


Figure 2.9: Visualisation of a PET detector with a gamma photon interacting with a crystal. The emitted scintillation light is spread over several sensors via the light guide which, in turn, lets each sensor generate one hit event.

ence on the throughput at the front-end of the acquisition system as the use of light-sharing increases the bandwidth requirements for more information to be read per time by the acquisition platform. If PET data is processed online during the acquisition, then the increased number of hits per single event might require additional computational resources for algorithms to determine singles from hits. Another influence on the throughput of a PET acquisition system is by the choice of radionuclide. A PET system to be used with short half-life tracers such as ^{15}O water for neurological studies or ^{13}N Ammonia for myocardial perfusion imaging

[52] with high tracer activities at the PET measurement start needs to be designed with a high maximum throughput.
Sometimes, the temporal and spatial propagation of the tracer is of interest and dynamic PET imaging is performed [53]. Here, data acquisitions with satisfactory tracer decay statistics in combination with short half-life tracers and short scan times require PET detectors and the acquisition system to support high coincidence rates.
The scanner geometry determines the geometrical efficiency which directly influences the bandwidth requirements of the platform, as radiation density at a PET detector is dependent on the solid angle, the latter being projected by the tracer activity source towards the PET detectors (see example in eq. (2.1) for an activity in the centre of the PET FOV).
The scintillation material choice has a direct impact on bandwidth requirements of an acquisition system. A higher stopping power of the scintillator yields a higher intrinsic detection sensitivity. The combination of a high stopping power e.g. via long crystals (in the radial direction) combined with low scintillation decay time properties leads to more dead time at high annihilation photon interaction rates.

2.1.4 Overview of state-of-the-art PET data acquisition architecture concepts

Most commercial PET/CT systems usually make use of a PET data acquisition system designed for the needs of the particular system and have little flexibility regarding modularity, scalability and data processing flavours depending on the type of system (preclinical or clinical). However, during the last ten years, data acquisition platform concepts and designs for PET scanners with a growing focus on digital data processing and with added flexibility have been proposed by academia and companies. Data acquisition and processing can nowadays be performed using components known as *field programmable gate arrays* (FPGA), which offer hardware logic that is reprogrammable at any time thus making its resources versatile and flexible. The possibility of using semiconductor-based photo-detectors with an increased number of channels compared to PMTs, combined with the computation power of current FPGAs has led to a generation

of new approaches for PET data acquisition architectures. They are designed for different purposes (e.g. clinical or preclinical), detectors, geometries and environments (commercial systems or research prototypes), while trying to cover requirements for different combinations of these. The structural and conceptual implementation approaches that describe the functionality and organisation of an acquisition platform are known as its *architecture*. In the following section, an overview is given of published PET data acquisition platforms, their similarities, and what the noticeable distinctions are.

PET data acquisition platforms presented during the last ten years with digital data transmission and processing approaches either make use of digital signal processors (DSP) [54], DSPs combined with FPGAs [55] or FPGAs, only [56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69]. DSPs are microprocessors with architectures optimised for the computation of digital signal processing algorithms. The interest in DSPs has, however, decreased since FPGA manufacturers started adding DSP blocks into FPGAs (covered in more detail in section 2.2). In some systems, the acquisition platform has the task of acquiring and concentrating detector data to be stored on disk. The actual coincidence processing is then performed offline (i.e. after data acquisition) using computer-based software [56, 66]. The primary advantage of this approach is the processing flexibility. With hits or singles data stored, data can be processed multiple times with different processing parameter settings or using completely different algorithms. Therefore, this approach is of interest particularly in the field of research and development [55, 61, 59]. A disadvantage is the potentially large amounts of data to be stored. The ratio of coincidence events and single events is usually not more than a few percent.

The majority of the acquisition systems cited above make use of a tree topology to connect so-called *processing nodes* which each other [55, 56, 57, 59, 66, 68, 69, 62, 64]. The implemented tree topology hierarchies vary between two and three levels between the front-end processing nodes at one end and the centralised node and the data storage at the other end. Using this topology type in combination with online data processing, the coincidence processing is usually implemented in the last node before data is stored on a computer [57, 68, 64, 62, 55]. Depending on the number of front-end processing nodes, an additional level in the tree is added in such a way that the number of channels and thus connections to the

coincidence processing unit are kept to a minimum [56, 55, 68].
As an alternative topology structure for acquisition platforms with digital signal processing, daisy-chain-ring topologies were presented by Siemens [60] (QuickSilver) and the University of Stanford [61]. Here, the nodes of the DAQ-architecture not only perform singles processing, but are also able to do Coincidence detection. The advantage of daisy-chain topologies is that a centralised, dedicated processing node for coincidence detection can be avoided by distributing this processing task over physical nodes all of the same type. This results in a cost reduction by avoiding dedicated hardware for a central node. However, there is a disadvantage to this approach: with an increasing number of nodes in a daisy-chain the coincidences processing throughput, at a fixed bandwidth of the node communication links, decreases. The approach of Stanford only allows a daisy configuration whereas the Siemens approach also supports tree-topology configurations [70].
A further development has been described by the SPADnet consortium where a multi-ring approach was chosen as an acquisition system topology [63, 71] with nodes being as small as the PET detector blocks and directly attached to them. The daisy-chains are of *linear* type (bi-directional communication between each node) in contrast to QuickSilver and the approach from Stanford which are daisy chain *rings* (uni-directional inter-node communication). The advantage of the multi-ring topology lies in scalability at a very small granularity level. However, for a larger clinical system, the small nodes would result in a very large quantity of interconnections, yielding a high number of connectors and cables. Moreover, the time stamp synchronisation of SPADnet is not performed via the multi-ring network, but via a separate, additional star-fashioned clock distribution network as reported in [72].
Some acquisition platforms separate, completely or in part, the communication path for PET data from the path for configuration, control and status data [56, 69, 62, 58]. This eases the communication-related implementation and avoids the need for additional, prioritisation-related precautions, if control- or status-related data is not to be affected by shared data links when the latter are saturated. The downside is a higher number of cables and components, which is a disadvantage when a very compact system design is required [73]. Some PET acquisition systems also offer gating inputs in order to add physiological and/or biological

information such as cardiac or respiratory cycles into the list mode data stream which can be taken into account during image reconstruction for artefact reduction [57, 55, 70, 74].

2.2 Field-Programmable Gate Arrays

Field-programmable gate arrays (FPGA) were introduced in the mid-1980s by Xilinx (Xilinx Inc, San Jose, California, USA). They are semiconductor devices whose integrated circuits are designed to be configurable "'in the field", i.e. after their manufacturing process at a customer's site. FPGAs can perform any kind of digital computation in terms of logic and arithmetic functions as long as the FPGAs have sufficient internal resources to be configured with a digital design specified by a designer or customer. The programmable functionality is obtained with *configurable logical blocks* (CLB) and a configurable interconnection system between the CLBs as shown in fig. 2.10.

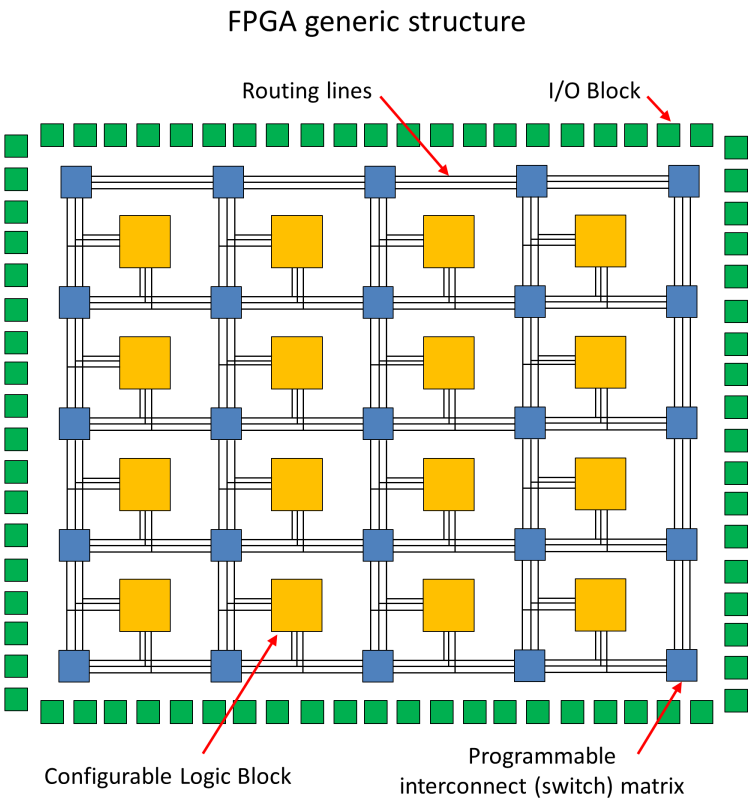


Figure 2.10: Generic structure of an FPGA: Configurable logic blocks offering programmable logic and registers can be interconnected with each other in versatile ways thanks to typically large amounts of routing lines spread across the device. Interconnections between the lines are defined using interconnect matrices. I/O Blocks are used to communicate with FPGA-external devices.

Figure 2.11 depicts a simplified CLB structure.

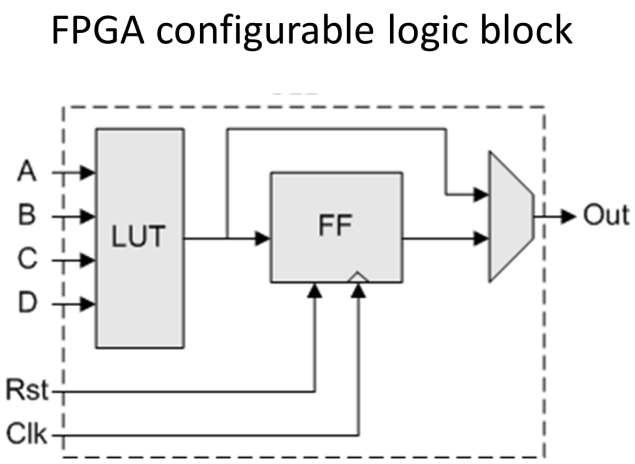


Figure 2.11: Configurable logical blocks typically consist of lookup-tables to implement combinational functions and memory elements implemented as flip-flops (FF). Figure taken from [75] (Creative Commons).

A CLB typically comprises one or more *Lookup tables* (LUT) and one or more registers serving as memory elements which are implemented as flip-flops (FF). LUTs consist of memory elements that are addressable by the LUT input ports. The LUT output value then presents a combinational function of the input ports depending on the LUT memory values stored, thereby making it possible to implement combinations of boolean operations such as AND, OR, XOR, NOT, NAND. The LUT output as a function of the LUT inputs is stored as a truth table in a LUT. An example for the function (a AND b) OR c is given in table 2.3.

As LUTs use memory to store truth tables, thereby acting as read-only memory (ROM), LUTs can sometimes also be configured to serve as small random access memories (RAM) depending on the FPGA device used. Registers serve the purpose of storing the combinational, non-clocked output results of LUTs. Registers map their input value to their output value at each rising edge of a clock signal. The output value remains stable during one clock cycle and is used to, e.g., feed inputs of further LUTs. The principle of registering results of combinational logic at each rising clock edge to serve as input to further combinational logic stages is the fundamental principle of digital, clocked designs.
Inputs and outputs of CLBs are connected with each other by large numbers of routing lines. Interconnection matrices as shown in fig. 2.10 are set up during

Table 2.3: Truth table for the combinational function (a AND b) OR c which can be stored in a LUT.

a	b	c	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

FPGA configuration to connect matrix inputs and outputs to obtain the desired connections between CLBs.

For applications requiring large LUTs, FIFO-memory or larger amounts of RAM, large memory blocks called *Block-RAM* holding 9, 18, 36 kBytes or more per unit are found in FPGAs in addition to CLBs. All memory elements (LUTs, registers, RAMs, interconnect matrices) of an FPGA consist of volatile static RAM. Therefore, after power-up of the device, every FPGA needs to be configured with the desired function known as a *firmware design*.

Nowadays, FPGAs are usually equipped with additional dedicated blocks which either offer accelerated computation power for particular operations, or add new functionality to CLB resources. Such dedicated blocks have a different structure to CLBs and are, compared to CLBs, not generically configurable and are therefore known as *hard macro blocks*, or hard macros. Common examples of hard macros are *digital signal processing* (DSP) blocks offering accelerated multiply-and-accumulate operations, multi-gigabit transceivers and high-speed serial link interfaces for FPGA-external communication, memory-controllers for external memory interfacing, as well as entire CPU cores. The functional blocks of FPGAs are commonly arranged in a columnar fashion on the silicon die to avoid bottlenecks regarding the accessibility between CLBs and the dedicated resources. An example of a block arrangement in a Xilinx Spartan-6 FPGA is shown in fig. 2.12

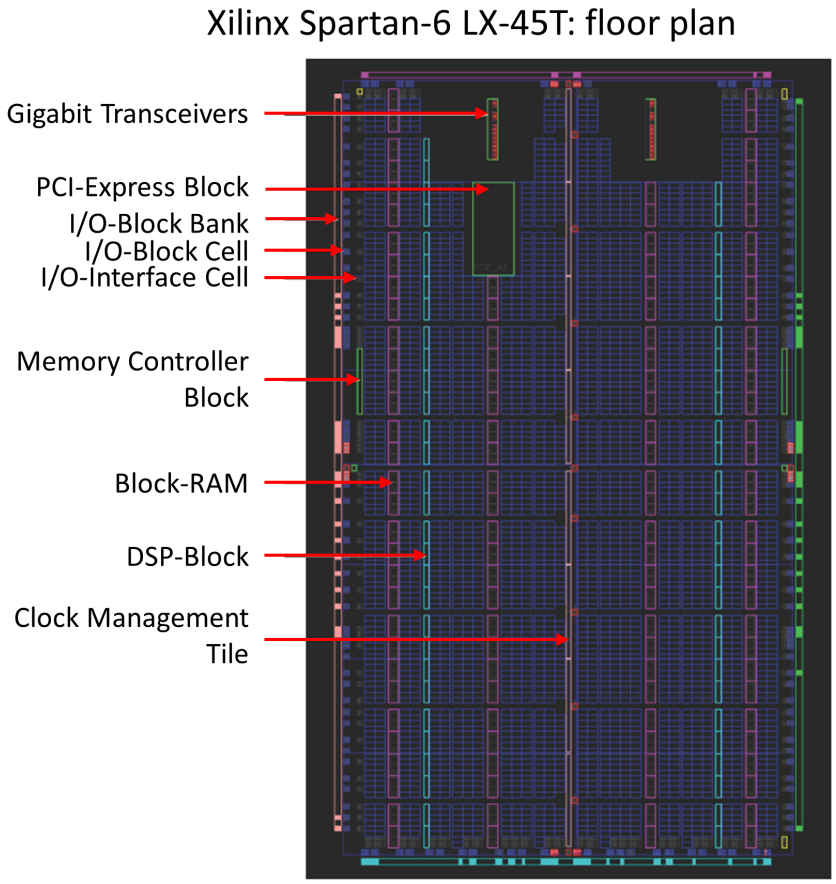


Figure 2.12: The columnar alignment of BlockRAM units, DSP blocks and clock management tiles is clearly seen in the floor plan of the Spartan-6 LX45T FPGA device. The example FPGA is equipped with further hard macros offering added functionality: two memory controllers, a PCI-express interface block and two multi-gigabit serial transceivers.

Dedicated functionality on top of CLB logic increases the application versatility of FPGAs which makes them suitable for a wide range of communication-intensive as well as computational-intensive tasks. Typical application areas are telecommunications, Aerospace, Medical and scientific instrumentation, consumer electronics. Another field of application is rapid-prototyping and ASIC development. Similarly to the functional design of ASICs, the firmware designs that FPGAs are configured with are written using *hardware description languages* (HDL) such as Verilog and VHDL.
The continuously increasing computational power in combination with the de-

creasing power consumption and small foot-print of FPGAs make them ideal for embedded data processing in highly integrated systems.

2.3 Magnetic Resonance Imaging

Magnetic resonance imaging (MRI) is an imaging modality based on a physical principle known as *nuclear magnetic resonance* (NMR). This principle was reported independently by Purcel and Bloch in the mid 1940s [76, 77], and it can be used to study the structure of chemical compounds by using NMR spectroscopy. In the 1970s, further research led by Lauterbur and Mansfield resulted in the first publications on NMR-based imaging techniques [78, 79]. Technical advancements in MRI devices and techniques have occurred over several decades to continuously improve the imaging capabilities and thus establish magnetic resonance imaging as one of the major imaging modalities in medicine. MRI allows anatomical structures to be imaged *in vivo* at very high spatial resolutions (e.g. for clinical systems in the range of 1 mm) and with a wide range of sources of contrast, particularly for soft tissues. In addition to anatomical imaging, MRI can be used to obtain functional information not only via spectroscopy, but also e.g. using diffusion or perfusion imaging, the latter two being important in the areas of neurological and cardiac MRI. *Functional MRI* (fMRI) is another MRI discipline in the area of neuro-imaging. It is based on changes in magnetic properties of oxygenated blood, thereby allowing the neural brain activity to be visualised by imaging blood flow changes. Besides *proton-based* (^{1}H) imaging, MRI can be used to visualise other nuclei such as ^{23}Na, ^{31}P, ^{17}O or ^{19}F. The former two are naturally present in bodies and can be imaged directly, whereas the latter are administered prior to the imaging procedure. An advantage of naturally non-occurring nuclei is the lack background (unwanted) signal which results in no loss of image contrast.

Compared to X-ray CT, MRI does not expose the patient to ionising radiation which is of particular interest in the domain of prenatal and paediatric imaging. Furthermore, MR imaging is characterised by superior soft-tissue contrast compared to CT.

2.3.1 Basic principles of MRI

Nuclear magnetic resonance is a phenomenon observed for nuclei with an odd number of protons and/or neutrons. These nuclei possess a spin angular momentum S that, in turn, creates a magnetic dipole moment

$$\vec{\mu} \ = \ \gamma \vec{S} \tag{2.3}$$

where γ is the *gyromagnetic ratio*. The latter is a nucleus-type-specific constant. The angular momentum is quantized, meaning that is can only have values within a restricted value range with discrete steps in between. Nuclei such as ^{1}H have two spin states with the states being approximately equally distributed among the nuclei with both spin states having the same energy. An exposure to an external magnetic field forces the protons to align either parallel or anti-parallel to the field. However, due to the Zeeman-effect, a difference in energy states is introduced and the nuclei in parallel alignment to the magnetic field experience a lower energy state than those in an anti-parallel alignment [80]. This yields a slightly larger number of protons to be aligned in the parallel compared to those aligned in the anti-parallel direction to the field which results in a net magnetisation with an amplitude proportional to the magnetic field in the case of body tissues. A *resonant absorption* of a photon with an energy equalling the difference in the two proton energy states allows the protons to transition between the two states. Photons with an energy matching the energy state difference are said to have a magnetic resonance frequency equalling the *Larmor* frequency.
In an MRI system, the static, homogeneous magnetic field $\vec{B_0}$ generated by MRI scanners is aligned with the head-foot direction of a patient which is defined as the z-axis. Nuclei in a patient's body tissue then align with the field and the resulting equilibrium leads to a net magnetisation $\vec{M_0}$ in direction of the $\vec{B_0}$ field. The spinning charge of the nuclei interact with the $\vec{B_0}$ field, thereby causing the nuclei to precess about $\vec{B_0}$ with angular frequency ω_0 equalling

$$\omega_0 \ = \ \gamma B_0 \tag{2.4}$$

, which is also known as the Larmor frequency. From eq. (2.4) it is seen that the stronger the B_0 field becomes, the faster the nuclei precess about the mag-

netic field. As an example, for ^{1}H nuclei, the Larmor frequency at 3 T equals 127.74 MHz. The magnetisation of the nuclei can be influenced by applying an electromagnetic field (in the μT range) perpendicular to the B_0 field via an RF coil. The magnetic component of an electromagnetic field tuned to the Larmor frequency will create a torque on the magnetisation $\vec{M}$ and rotate it away from the direction of B_0. As only the magnetic component is of significance for the rotation with the Larmor frequency lying in the *radio-frequency* (RF) range, this field is usually referred to as the RF field or B_1 field. The *flip angle* α between the z-axis and the rotated magnetisation vector depends on the electromagnetic field strength and the duration of the applied field. The application of an *RF pulse* for a short amount of time for the purpose of the magnetisation rotation is known as *excitation*. Generally, the magnetisation vector consists of a longitudinal component $\vec{M}_z$ and transverse component $\vec{M}_{xy}$. The former decreases, and the latter becomes non-zero and increases when the rotation begins. Rotating the longitudinal magnetisation into the transverse plane so that $\vec{M}_z$ ideally turns to zero maximises the transverse magnetisation. This is obtained by applying RF pulse yielding a flip angle of 90°. An angle of 180° inverts the longitudinal magnetisation $\vec{M}_0$ which is why the RF pulse applied to obtain an inversion is called an *inversion pulse*.

Following the excitation, a process known as the *relaxation* occurs during which the nuclei return to their original equilibrium. During this process, the longitudinal magnetisation re-establishes while the transverse magnetisation decreases towards zero. The speeds, at which $\vec{M}_z$ increases and $\vec{M}_{xy}$ decreases, are independent of each other [81]. The longitudinal relaxation is based on an energy exchange between the nuclei and surrounding lattice and is characterised by the time constant T_1. The transverse magnetisation decreases with time due to energy transfers between neighbouring nuclei. These interactions lead to changes in the nucleis' spin orientation which introduces fluctuations in the resulting precession frequencies, causing a gradual loss of phase coherence between the spinning nuclei. This leads to a decrease in the transverse magnetisation and the velocity of the decrease is characterised by the time constant T_2. Due to inhomogeneities of the $\vec{B}_0$ field causing nuclei to precess under slightly different frequencies, the phase coherence loss during the transverse relaxation is accelerated and this is taken into account by the time constant T_2^* with T_2^* being smaller or equal to T_2.

During the processes of excitation and relaxation, the magnetisation vector precesses with the Larmor frequency about the B_0 field due to the torque between the two fields. The oscillating transverse magnetic component of the magnetisation vector represents a time-varying magnetic field. Through Faraday's law of induction, a coil exposed to a time-varying field will experience an electromagnetic induction in form of voltage between the ends of the coil wire. The voltage measured by an *RF receive* coil located near the sample or volume of interest represents the *MR signal*, and the signal shape is described by the *free induction decay* (FID). The usually weak MR signal is pre-amplified after reception and is then digitized, followed by signal processing and MR image reconstruction. The RF coil used to transmit an RF pulse for RF excitation purposes may also be used to receive the MR signal during relaxation, as it needs to be tuned and thus be resonant at the Larmor frequency for RF transmission and reception.
The received FID signal as such does not contain any spatial information, as all nuclei spin with a similar Larmor frequency within the homogeneous B_0 field. By applying linear gradient fields over the B_0 field in the axial(z) and the two transverse (x, y) directions, a 3D spatial encoding can be obtained using three independent *gradient coils* G_x, G_y, G_z. As a first step, an image *slice* is selected by applying a slice-selection gradient oriented perpendicularly to the slice during RF excitation. MRI systems not only excite with one frequency, but rather with a narrow B_1 frequency range. The linear gradient applied during RF excitation causes only the nuclei within a single slice to be rotated, or flipped. By varying the gradient amplitude, the slice thickness can be varied. Once the slice has been selected, the slice plane itself needs to be spatially encoded. As an example, if a slice is selected with the G_z gradient, further encoding steps in the x and y directions are performed. By shortly applying the *phase-encoding* gradient, the nuclei are increased or decreased in frequency depending on their location in the gradient amplitude during gradient application. After deactivation of the gradient, the nuclei spin at the same frequency again, but with fixed phase differences to each other, allowing their location to be uniquely encoded. Encoding in the second transverse direction is realised with the frequency-encoding gradient (or *readout* gradient). It is applied during RF signal reception, causing the nuclei to precess at different frequencies. The location is then determined via the received frequency and the applied readout gradient amplitude.

2.3.2 MRI system overview

Figure 2.13 shows a simplified overview of the basic components of an MRI system.

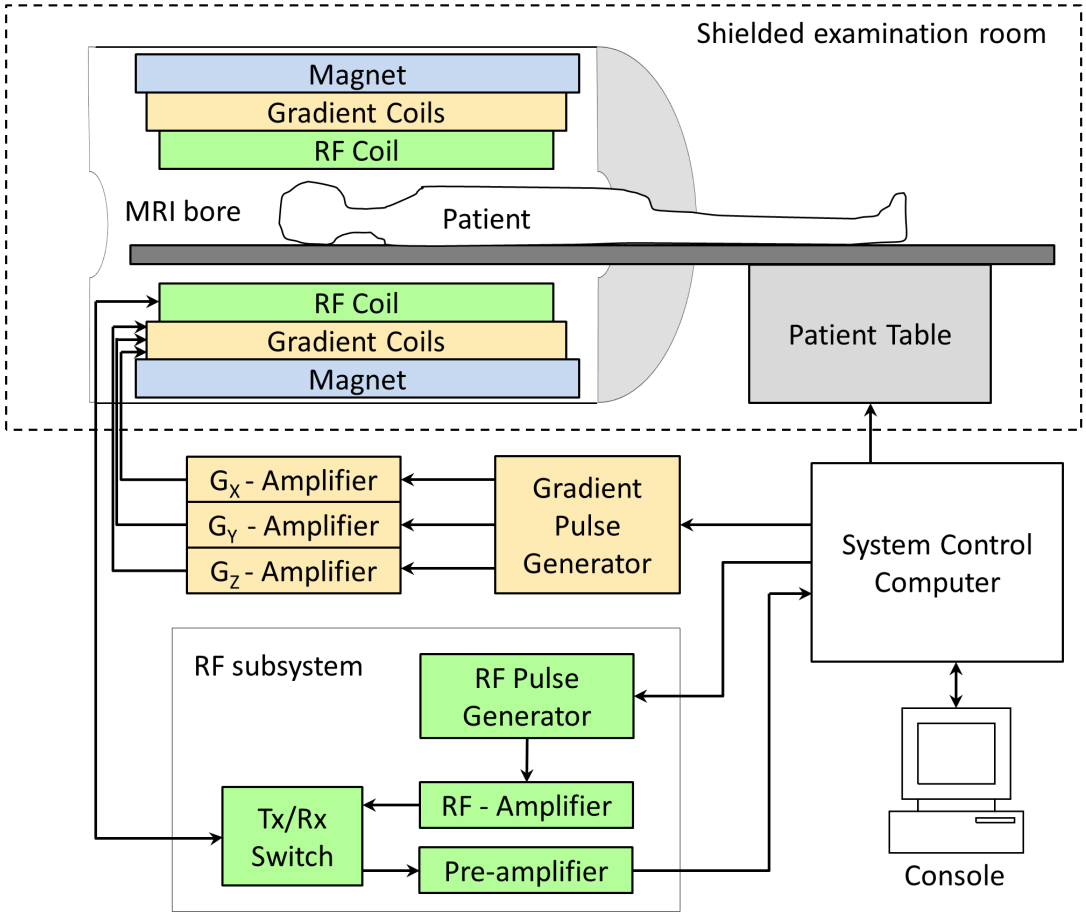


Figure 2.13: Simplified overview showing the basic components of an MRI scanner.

The MRI scanner consists of a large gantry with a bore to accommodate the patient (clinical whole-body (WB) MRI) or small animals (preclinical MRI) to be scanned. The gantry contains the main *magnet* that generates the static and homogeneous B_0 field inside the bore. Clinical systems are nowadays usually equipped with superconducting high-field magnets which need to be permanently cooled with cryogens. The requirements of main magnets are to provide for a highly homogeneous field with maximum fluctuations in the area of a 2 to 3

parts per million (ppm). Inhomogeneities result in impaired MR image quality due to distortion-related artefacts. The magnetic fields applied by *whole-body* (WB) MRI systems used for clinically approved diagnosis vary between 1 T and 4 T. WB-MRI scanners used for research are available at 4, 7 and 9.4 T. Preclinical MRI scanner cover a field strength range up to 21.1 T.

The three independent gradient coils used for spatial encoding are located between the magnet and the RF coil. They operate in the kHz-range and are designed with highly demanding specifications with respect to the field linearity and accuracy of field slopes. Distortions in the gradient field amplitude result in encoding disturbances, leading to a degradation in MR image quality. As shown in fig. 2.13, a pulse generator implements the gradient pulses as required for the MR sequence execution and FOV selection. These pulses are then amplified by powerful amplifiers to deliver currents in the range of hundreds of amperes.

The RF coil is located at the inner-most position in the bore, in case of a whole-body RF coil. Additionally, dedicated coils optimised e.g. for brain, cardiac, knee and breast imaging are available and located as close as possible to the volume of interest to receive as much RF signal as possible. Some coils are dedicated receive coils, whereas some offer the possibility to transmit as well as receive RF signals. Different approaches to RF coil design have been proposed over the decades and a detailed overview is given by [82]. Generally, an RF pulse generator in the MRI system forwards the pulses used for excitation via amplifiers to the RF coil. When the MRI switches to receive mode during MR signal readout phase, the usually weak MR signals are first pre-amplified before undergoing digitization and processing. Any unwanted disturbances in the RF range can negatively affect the MR image quality. The image quality is determined by its SNR and a low MR signal-to-noise ratio directly affects the image SNR. The MRI SNR can be improved by longer scan times and depending on the type of examination by the use of MRI contrast agents. These are administered and provide an MR signal increase.

The examination room containing the MRI bore is always RF-shielded to protect from external RF noise.

2.4 Hybrid PET/MRI

The introduction of combined PET/CT systems in the late 1990s [1] allowed the improved diagnostic accuracy obtained via anatomical high-resolution information from CT and metabolic information from PET to be demonstrated. Patient study results yielded benefits especially for cases of uncertain diagnosis which were resolved thanks to a more precise localisation of physiological lesions obtained with CT information [4]. The added value lies in the complementary information provided by CT and therefore, PET/CT became quickly established in both nuclear medicine and radiology environments. Similarly to CT, MRI offers high-resolution *in vivo* anatomical imaging, but without any ionising radiation, which is of particular interest for prenatal and paediatric imaging,, and MR-guided disease therapy monitoring. The high soft-tissue contrast and the possibility of providing for functional information via spectroscopy-, perfusion- or diffusion-imaging distinguish MRI from CT, thereby offering a different type of complementary information when combined with PET. Moreover, simultaneous image acquisition leads to highly accurate spatial and temporal registration of PET and MRI data. This potentially offers a quantitative accuracy increase of PET images via MRI-based motion correction of PET data [83, 84, 85, 10]. The combination of functional MRI and PET may lead to new applications by temporally correlating their data sets [6, 86] or by combining PET and MR spectroscopy [87, 5]. Clinical diagnosis or therapy employing both MRI and PET can suffer from long procedure times. A simultaneous imaging approach would accelerate the work flow and be advantageous particularly with regard to paediatric, fragile or older patients.

This and the rise of improved and new technologies motivated research groups and companies to address the topic of designing PET detectors to be integrated into MRI systems. An integration of a PET system into an MRI scanner not only requires a PET detector to be very compact to fit into an MRI while offering a combined FOV large enough to image humans in case of clinical MRI or small animals in case of preclinical MRI. It also requires the PET and MRI systems to be designed in such ways that they offer a simultaneous bi-modal image acquisition with the intrinsic imaging performance remaining unaffected. This is important, as unwanted interference between the two image modalities may lead to impaired

image quality on either side. The different types of interferences affecting the bi-modal operation are described in the next section.

2.4.1 Interference between PET and MRI

The types of interference, which can occur between PET and MRI, are (static and dynamic) magnetic- as well as electromagnetic-field-related and are as follows:

1. Interference introduced by PET which may disturb the MRI operation:
   (a) PET detector materials have a non-zero susceptibility, in particular ferromagnetic ones. This locally distorts the MRI B_0 field homogeneity and leads to image artefacts.
   (b) Eddy currents induced in PET detectors disturb the MRI gradient fields spatially and temporally, resulting in MRI spatial encoding distortions.
   (c) Depending on the PET detector design, electromagnetic RF fields may be emitted within the MRI bore. This RF radiation can couple into the MRI RF coil and affect the MRI SNR, thereby leading to a deteriorated MRI quality.
2. Interference introduced by MRI which may affect PET operation:
   (a) The strong MRI B_0 field can either lead to a disturbed operation of electronics (e.g. Hall effect) or prevent operation altogether (saturated coil ferrites or Lorentzian forces on electrons in PMTs).
   (b) The time-varying MRI gradient fields generate eddy currents in cables, printed circuit board (PCB) traces as well as conducting areas. This may cause electronic signal disturbances,physical stresses and material heat-up.
   (c) RF pulses generated by the MRI RF coil during excitation phase can induce eddy currents and voltages in conducting areas, cables and PCB traces. Again, electronic signal disturbances may occur.

PET detectors are said to be *MR-compatible* if they are capable of being operated within or in close proximity to an MRI bore. However, interference

may still occur and remaining interference between PET and MRI determine the degree of MR-compatibility.
Since the presentation of the first PET/MR prototype systems in the 1990s, different design concepts and implementations for hybrid PET/MRI have been proposed by academia and industry. The next section gives an overview of some of these.

2.4.2 PET/MRI systems overview

The earliest prototypes designed to demonstrate simultaneous PET/MR imaging were reported in the second half of the 1990s prior to the emergence of the combined PET/CT system. These were namely the McPET [88] and McPET-II (or PANDA) PET inserts [13, 14, 89] that aimed at preclinical imaging. The advantage of an insert placed into an MRI bore is that the MRI does not need any technical modifications for the operation with the PET insert (see fig. 2.14(b)). The aforementioned inserts use *lutetium oxyorthosilicate* (LSO) scintillation crystals that are optically coupled via 4-metre-long optical fibres to PMTs. The crystals and fibres are unaffected by the MRI fields and the scintillation light is transmitted to PMTs located sufficiently far away from the MRI bore. The distance avoids magnetic-field-related interferences which may prevent PMT operation. The McPET and PANDA inserts were successfully operated in 9.4-T Bruker NMR and 1.5-T clinical MRI systems. The disadvantage of the optical coupling technique with fibres lies in the fractional resulting loss of scintillation light, leading to a reduction in timing and energy resolution and crystal identification accuracy. Another drawback is the number of optical fibres which only allows for a limited scalability. To my knowledge, no clinical PET ring configurations were designed using PMTs with attached optical fibres. The main advantage of this PET detector design is the use of well-established PMT technology with low-noise and high-gain properties. They can be combined with off-the-shelf electronics for PET signal processing. This is one of the reasons why other research groups followed this PMT-optical-fibre-combination approach in later years [90, 91, 5, 92, 93].
The PET/MRI systems reported in [94] and [95] also make use of PMTs coupled to optical fibres, but the PET system is not designed as an insert. Instead, the scintillator and fibres are fully integrated in the MRI bore and the MRI systems

rely on newly developed split-magnet MRI and field-cycled MRI designs. The idea of alternative MRI system designs to integrate a PET detector did, however, not spread, which is most likely related to the complexity and costs related to an MRI system re-design.

Two sequential clinical PET/MRI systems were introduced to the commercial market by Philips (Philips Healthcare, Best, the Netherlands) and General Electric (GE Healthcare, Waukesha, WI, USA) and imaging results were published by [96, 97] and [98], respectively. In both cases, the PMT-based PET system is located on a separate gantry sufficiently far away from the MRI bore to remain unaffected (i.e. by the fields in the proximity of the MRI bore). As shown in fig. 2.14(a), both systems share a common patient bed to reduce image artefacts related to a patient displacement. However, the sequential imaging approach and patient movement on the bed can still lead to image registration artefacts. Moreover, the installation of such systems requires a lot of space and the sequential imaging procedure yields long scan times compared to PET/CT. Whereas for PET/CT, a CT scan takes less than a minute compared to a typical WB PET scan with several bed positions of 2-3 minutes typically taking around 20 minutes, an MRI scan can easily take 20 to 40 minutes.

A third commercial solution with a sequential approach using magnetically shielded PMTs was presented by Mediso (Mediso Medical Imaging Systems, Budapest, Hungary) as the nanoScan preclinical PET/MRI. With a PET resolution of 0.91 mm FWHM (iso-centre) and a peak sensitivity of 8.41 %, the PET subsystem belongs to the best performing preclinical PET systems available [65]. However, truly simultaneous imaging is not possible, thus limiting the range of applications.

As introduced in section 2.1.2, semiconductor-based avalanche-photo-diodes (APD) and silicon photo-multipliers (SiPM) can operate in strong magnetic fields. Therefore, these are very suitable for PET detectors to be operated in an MRI environment [38]. Several PET detector systems for PET/MRI based on APD technology haven been reported over the last 10 years. First PET/MR interference and performance studies with one PET detector *module* or two opposed modules were presented by UC Davis jointly with the University of Tuebingen [99], and Siemens [100], respectively. These served as preliminary studies on the way to two PET inserts with full-ring configurations, one from UC Davis [101] and the other one

from Tuebingen [102, 6]. Both systems were designed to fit into 7-T preclinical MRI systems (Bruker Corp., Billerica, Massachusetts, USA). The insert from UC Davis coupled the LSO crystals via short (10 cm) fibres to the APDs and front-end analogue electronics with the idea of placing the electronic components outside the MRI FOV to preserve MR image quality as much as possible. As the electronics were still located in the MRI bore, they were RF-shielded to avoid potential, mutual RF interferences.

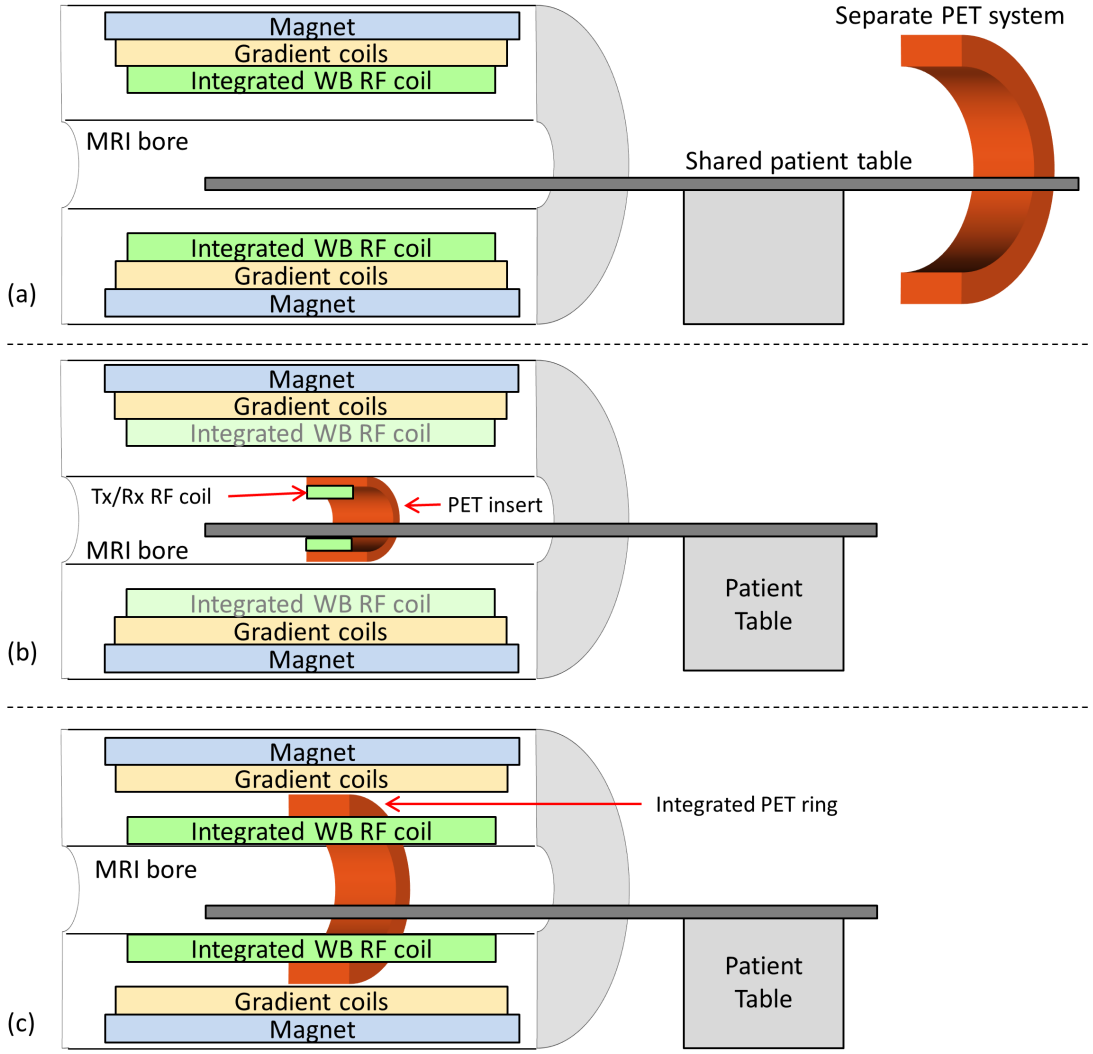


Figure 2.14: Schematic overview of PET and MRI system arrangements for hybrid PET/MR imaging. In (a) is shown a sequential alignment with the two modalities sharing one patient bed. (b) depicts a PET system that is fitted into the MRI bore and a separate RF coil. In (c) is shown an integrated device, where the PET system is fully integrated into the MRI.

The scintillators used for the insert from Tuebingen were coupled via a small light guide to the APD sensors. Both inserts were studied [103, 104] regarding PET/MR interference and both systems showed little PET and MR performance degradation with respect to the applied MR sequences. In addition to the aforementioned drawbacks related to limited system scalability with optical fibres and bending-related light loss, the high temperature changes in the MRI bore due to

operating the PET insert under insufficient cooling capabilities resulted in MRI mean signal changes [104]. This outlines the need for a stable temperature environment for simultaneous PET/MR imaging, not only for a stable gain of the PET photo-detectors, but also e.g. for MR spectroscopy measurements which are temperature-sensitive. Adequate cooling control becomes more important, the more PET-related materials (with potential eddy-current-related heat-up) and electronic-related heat-dissipation are located in the MRI.

Other examples of built and well-studied, APD-based PET inserts for PET/MR imaging are based on the ratCAP PET design [105]. These inserts use LSO crystals coupled via a small light guide to APDs and APD signals are digitized by dedicated low-power ASICs having a small foot-print to allow for a compact PET detector design. Several versions were adapted and built for small animals in a preclinical 9.4-T MRI scanner [106, 107, 108] and clinical 4-T MRI system [109] or for breast PET/MR imaging in a clinical MRI system with the PET ring having no RF shielding [110]. In the latter publication, it was reported that RF interference, which originated from long power cabling to the PET insert, coupled into the MRI RF coil and thus led to image artefacts. In [111], it was observed that MRI-related RF interferences lead to eddy-currents in the RF shielding of the PET detector modules, which, in turn, degraded the PET performance. Tests with continuous aluminium RF shielding of the PET detector led to eddy currents, thereby impairing the MR image SNR. The shielding was optimised using segmented copper which led to a good trade-off between PET and MRI performance, but a PET performance impairment during MRI RF excitation was still observable for some of the MR sequences chosen by the authors. The solution was to gate PET data during MRI excitation which, however, decreases the mean PET sensitivity due to less acquired coincident prompts. Apart from the aforementioned RF interference observations, these inserts provided a reasonable performance for most of the MR sequences tested.

Several APD-based PET inserts for simultaneous PET/MR brain imaging were built and investigations were published by [86, 112]. These systems revealed PET coincidence-rate-related issues (loss of approx. 3%) for standard as well as fast-gradient-field-switching echo-planar-imaging (EPI) sequences. PET-related RF interference led to a small MRI RF noise level increase. However, brain studies using PET combined with fMRI or spectroscopy were successfully performed with

only small performance degradation [86].
The first commercially-available, simultaneous, clinical PET/MRI was developed by Siemens with 80 installations world-wide [113] and its performance was first reported in [114]. The MRI system was modified to house an APD-based PET subsystem which is fully integrated into the MRI. The arrangement of the PET detector and the MRI coils is shown in fig. 2.14(c). The two subsystems can be operated independently and the initial performance results showed that an integration of PET detectors very close to the gradient and RF body coil does not lead to PET or MRI performance degradations. Due to the use of APD sensors, the system coincidence timing resolution is around 3 ns and therefore does not enable Time-of-Flight measurements.
Only a few years later after the rise of APD-based PET research prototypes for PET/MRI, the first SiPM-based PET systems such as the Hyperion-I PET insert were presented [115]. With this preclinical insert, the digitizing PET electronics were moved closer to the PET SiPM sensors with the aim of preserving the PET signal SNR. Moreover, it allowed concentration of the high number of 3840 SiPM channels resulting from the large axial 9-cm FOV into a few data lines as early as possible. More details about the insert are presented in section 2.5. In [116] and [117], the PET and MRI performances were assessed and revealed a very low MRI B_0 disturbance (< 2 ppm), and a reduced MRI SNR of up to 14 %. The PET timing and spatial resolution remained unaffected during MRI operation and only the coincidence rate was reduced by 2% during a 3-minute-long EPI MR sequence. The coincidence timing resolution of 530 ps [115] measured during the MRI operation demonstrated that SiPMs are in principle suitable for ToF-based PET/MR imaging.
An SiPM-based PET insert prototype for human brain PET/MR imaging was built by the University of Sogang [118, 119]. The PET FOV has a diameter of 39 cm and is 6 *cm* long in axial direction. The design approach was to minimise the amount of PET detector electronics in the MRI bore. Therefore, analogue signals from the 4608 detector channels (18 detector modules with 256 SiPM-channels each) are transferred over 4-m-long shielded flat cables to shielded electronics residing outside of the MRI bore but within the MRI examination room. Studies with a phantom showed that MRI SNR was reduced by up to 7 % which was likely caused by eddy currents induced in the PET gantry shielding. Due to MRI

RF interference, the PET coincidence timing resolution decreased by 6 %, and the count rate by 2 %, but the PET performance was reported to be otherwise satisfactory during simultaneous PET/MR imaging.

All formerly presented PET/MR configurations make use of specially designed MRI RF transmit/receive coils located inside the PET FOV to maximise the MRI SNR. With a densely-arranged PET detector ring (often with RF shielding) within the RF transmit coil FOV, the MRI SNR would suffer from a strong attenuation of the RF signal by the PET ring on the way to the combined FOV. However, two PET insert design approaches were presented with that they used the built-in MRI clinical RF body coil rather than building an expensive dedicated Tx/Rx coil. Both the PET inserts from the University of Seoul [120] and the one from Stanford [121] are SiPM-based. Short fibre bundles are used by [120] between the lutetium yttrium oxyorthosilicate (LYSO) scintillators and the SiPMs in the radial direction. This results in a gap for RF pulses from the RF body coil to pass easily towards the combined PET/MRI FOV. A simple RF surface receive coil was placed in the combined FOV. The SiPM signals are transferred outside the MRI examination room using shielded twisted pair cabling.

Stanford used battery-driven electro-optical coupling to transfer the SiPM signals optically via 256 fibres from the human-brain PET insert to front-end electronics outside the MRI room. The PET modules are shielded with copper and are electrically floating with respect to MRI RF ground, thereby acting as a Faraday cages. This allows RF pulses to penetrate into the combined FOV and to use an RF coil solely for MR signal receive purposes. For standard MRI gradient echo (GRE) and spin echo (SE) sequences, count rate losses were observed, leading to a sensitivity drop of up to 11 % due to MRI RF interferences. An MRI SNR loss between 38 % and approx. 50 % was measured for the test MRI sequences due to the RF shielding of the PET modules [121].

GE have also presented a clinical PET/MRI system offering simultaneous image acquisition [122]. Similar to the Siemens mMR, the PET system is fully integrated in the MRI and signals from SiPMs are locally digitized using dedicated ASICs. The PET system is TOF-capable and first performance measurements showed only a negligible PET timing resolution degradation during MRI operation. The PET performance was said to not lead to MR image quality degradation.

In 2012, the successor of Hyperion-I was presented as a result of a joint collabor-

ation by Philips, the University of Aachen and King's College London [123]. The main difference between the two inserts is related to the SiPM technology. For Hyperion II^{D}, analogue SiPMs were replaced by digital SiPMs. The PET gantry uses similar dimensions and the same number of PET modules as Hyperion-I, but numerous electronic and mechanical improvements were performed to increase the PET system performance and decrease PET/MRI interference. More details will be presented in section 2.6. Apart from a coincidence timing resolution increase of 6 ps during EPI sequence execution, the PET performance parameters were not degraded by any of the tested MRI sequences. With an RF Tx/Rx coil for mouse imaging, the MRI SNR is decreased by up to 5 %.

2.4.3 RF interference reduction

A major aspect of PET/MRI design strategy is the PET signal transmission away from the PET ring to the location where the PET signals are processed by front-end electronics, followed by digital signal processing. Two major trends can be observed. In one case, the photo-detector signals are sent over shielded cabling or optical fibres from the MRI bore to an outside location to be digitized and processed [102, 108, 86, 120, 124, 118, 121]. In the other case, the analogue photo-detector signals are digitized (and processed) within the MRI bore [109, 117, 125][107, 108, 126][38, p.R140-R141]. To better understand advantages and drawbacks of both approaches, the following paragraphs introduce some basics related to analogue and digital signals, transmission standards, and the impact on these of time-varying magnetic fields including the electromagnetic ones.
Electrical signals transmitted through signal lines can experience crosstalk when being close to each other. They can also suffer from disturbances when they are exposed to externally-sourced, time-varying magnetic fields. Both cases yield unwanted disturbances in terms of signal quality degradation, or in other words known to generate noise. An analogue signal has continuously varying values with respect to amplitude and frequency. The transmission of analogue signals, such as those generated by APDs and analogue SiPMs, usually requires a pre-amplification step in order to increase the signal gain. This is done by amplifying the shape of the input signal to obtain the same shape at the amplifier output. Any noise added to the signal on the way to the amplifier will therefore be ampli-

fied, too. Therefore, specially designed low-noise amplifiers are used for analogue signal amplification of semiconductor-based photo-detectors in PET to minimise the potential of added noise [127, 128, 129, 130, 43, 131, 41, 132]. A possibility to filter noise from signal information regardless of the noise amplification can be obtained by encoding the analogue signal information digitally, i.e. using different, discrete signal amplitude levels. The well-known example is binary encoding using two discrete signals with margins and a threshold between the latter. Amplitudes below the threshold represent the logical Zero while amplitudes above the threshold stand for the logical One. The binary value of a signal with noise can be correctly assigned as long as the distorted signal is within the margins [1]. Then, the digital signal of a sampled signal can be cleaned by recreating it at any time without recreating its noise as visualised in fig. 2.15.

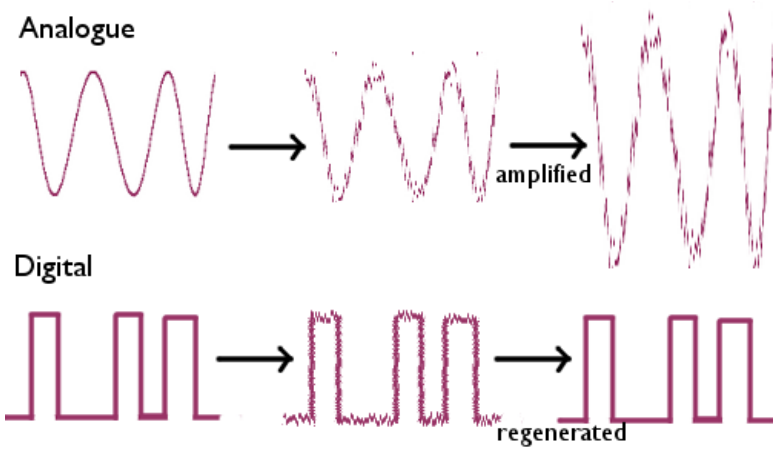


Figure 2.15: Any noise picked up during the transmission of analogue signal information is amplified together with the desired signal by amplifiers. Using digitization, the desired signal information can be separated from the noise via signal recreation. Figure taken from [133].

In the previous paragraph, a way to deal with noisy electrical signals was demonstrated. In the following, two common signal transmission types are introduced and discussed with regard to the influence on noise pick-up during signal

[1]For technical reasons, digital circuits actually use two thresholds, a lower for the binary Zero and an upper threshold for the binary One. Signal levels between the two are considered invalid

transmission and how this can be reduced.
Commonly, transmission of electrical signals is performed by using one signal line per information channel between a source and a destination. The electrical return path is, however, shared by many channels. Known as *single-ended* signal transmission [134], this transmission type offers high integration density, is cost-effective and therefore wide-spread. However, when fast, high-bandwidth signal switching is applied, the lines tend to emit electromagnetic (EM) fields. They are also prone to EM field reception which leads to noise pick-up during signal transmission. Additionally, as the signal line forms a closed area (via a closed loop) with the return path which is not spatially adjacent to the signal line, noise is induced in the lines when the area is exposed to time-varying magnetic fields due to Faraday's law of induction. Differential signalling techniques such as *low-voltage differential signalling* (LVDS) are less prone to these effects, as they use a dedicated closed-loop path for each information channel with opposed voltage levels on each line. The lines are usually placed adjacently which minimises the area within the closed loop, thereby making them less sensitive to induced noise pick-up. The opposed voltages in both lines lead to an opposed current flow at same magnitude. Therefore, the equal EM fields generated by the lines are also opposite to each other and tend to cancel out. Differential signalling requires more space on circuit boards and dedicated electronic components and thus is sometimes not an option for designs that are subject to severe space restrictions.
The above-described effects caused by MRI RF pulses and switching gradients fields can degrade PET performance, which was for instance reported in [112, 135]. These effects can, however, also be used intentionally. In [136], the successful temporal synchronisation of the PET and MRI systems was reported, which was achieved by adding time stamps to the PET data stream whenever gradient-switching occurs. These works are not based on eddy currents induced in the PET signal data path, though. In summary, a reduction of MRI-field-related disturbances along the PET signal acquisition path can be obtained by digitizing any PET signal information located in or close to the MRI bore. The earlier a digitization takes place, the higher the probability of preserving the intrinsic PET signal SNR and the related performance, which increases the *MR compatibility* of a PET system.
Digital signal transmission and additional electronics needed for digitization and

digital data processing within or close to the MRI, however, can increase interferences detected by the MRI as listed in section 2.4.1. Periodic signal switching as used for digital electronics or frequent signal switching for signal information transmission particularly over single-ended cables and PCB traces let the latter act as antennae [137]. The resulting EM fields with frequencies in the RF range can couple via the MRI RF coil into the MRI RF chain as noise and deteriorate the MRI SNR. Many observations of this have been reported [138, 124, 108, 111, 139, 117]. To suppress the unwanted, PET-related RF signal coupling, EM interference (EMI) shielding techniques are commonly applied to all electronics and cables in the MRI environment [102, 103, 140, 141, 111, 124, 118, 117, 125].

2.5 PET insert *Hyperion I*

2.5.1 Introduction

In 2009, the development of the SiPM-based, preclinical PET insert *Hyperion I* for simultaneous PET/MR imaging was presented [115]. These works were a result from joint efforts driven by a European collaboration of academia and industry called *HYPERImage*[2]. The PET insert served as a feasibility study to demonstrate the suitability of SiPMs for time-of-flight PET/MR imaging. At this time, previous full-ring PET prototypes with semiconductor-based photodetectors used APDs. The results and experiences gathered with Hyperion I were to be used for future clinical whole-body PET/MRI systems.

2.5.2 PET insert design overview

The PET ring consists of ten PET detector modules referred to as *Singles Detection Modules* (SDM). They are mounted on a gantry which was designed to fit into a clinical 3-T MRI (Philips Achieva 3T, the Netherlands). The PET data acquisition design follows the approach of digitizing all PET detector signals as early as possible within the SDMs in order to prevent MRI-related interference from negatively affecting the PET SNR. Each SDM houses up to six detector stacks in a 2×3 arrangement, thereby forming from one to three PET detector

[2]HYPERImage was an European FP7 project, grant agreement no. 201651

rings. Figure 2.16(left) depicts an open SDM equipped with two detector stacks. The structure of one detector stack is shown in Figure 2.16(right) as an exploded view. An LYSO crystal array composed of 22 × 22 crystals for the outer rings (22 × 24 crystals for the inner ring) with a crystal pitch of 1.3 mm × 1.3 mm × 10 mm is optically coupled via a 1.5 mm-thick glass plate to a sensor board. The latter is equipped with 16 monolithic 2 × 2 SiPM arrays yielding 64 individually operating SiPMs. The SiPM signals are transmitted via differential lines

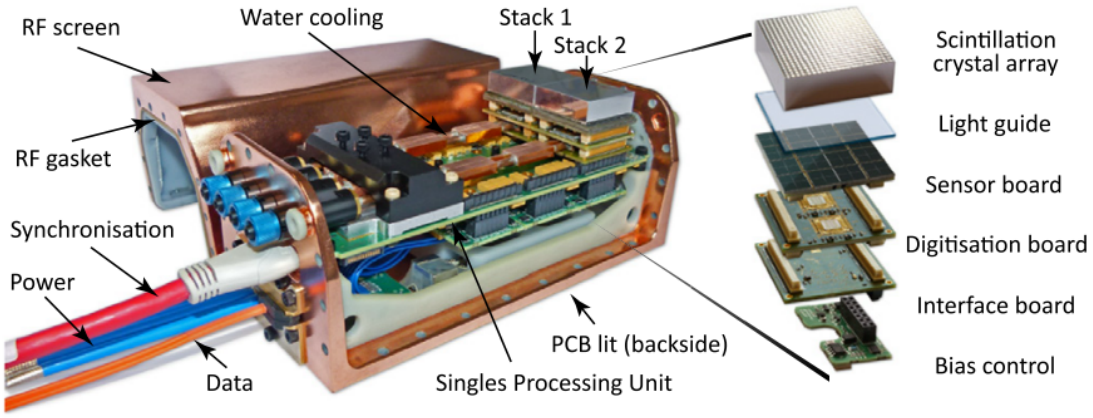


Figure 2.16: Left: Singles Detection Module equipped with two detector stacks and with removed RF screen. Right: Exploded view of a detector stack. Figure reprinted from [117]. © Institute of Physics and Engineering in Medicine. Reproduced by permission of IOP Publishing. All rights reserved.

(LVDS) to the digitization board which comprises two ASICs. Every ASIC has 40 SiPM channel inputs of which 32 are actually connected to SiPMs [41]. The remaining channels are used as spare or sync-channels for system-wide temporal (time-stamp) synchronisation purposes. The ASICs measure the energy provided by the SiPM pulses, perform time-stamping using time-to-digital converters and add channel identification information to the digitized photo-detector data. The hit (or raw) data from all input channels of both ASICs is read out digitally via six LVDS lines by an FPGA of type Xilinx "Spartan-3e" residing on the interface board.

The stacks are connected to the *Singles Processing Unit* which represents the main board of the SDM. There, an FPGA of type Xilinx "Virtex-5" communicates with the stack FPGAs via point-to-point links and forwards all data over a Gigabit Ethernet link to a data acquisition and processing server system where

all PET data sets are eventually stored [142].
The temporal synchronisation needed for PET data processing and coincidence detection is realised via a 625 MHz clock signal through the synchronisation cable (see fig. 2.16(left)) and referred to as the *reference clock*. The reference clock drives 15-bit-wide coarse counters resulting in a time window of 52.43 μs before they overflow. The time within one coarse count period of 1.6 ns is determined with the TDCs which have an average time resolution of 50 ps. To accurately synchronise the FPGAs with the ASICs, given that such a high frequency of 625 MHz is not supported by the FPGAs, the reference clock signal is divided by four using an external clock divider chip.The time range beyond 52, 43 μs is covered by the FPGAs by extending the time range using a further 32-bit-wide counter which counts the coarse counter overflows, yielding in a PET system time range of 2.6 days.
The large amount of electronics lead to a power dissipation of approx. 37 Watts per SDM. Therefore, a combination of water- and air-cooling is provided. All ten SDMs are mounted on a gantry as shown in fig. 2.17. The gantry is fixed on a supporting frame together with a *central synchronisation unit* (CSU) which generates and provides the reference clock and synchronisation signals to all SDMs for the system-wide temporal synchronisation and synchronised start and stop of the PET data acquisition. The supporting frame with the gantry and the CSU are placed on the MRI patient bed with the power supply and the cable carrier located next to the MRI table.

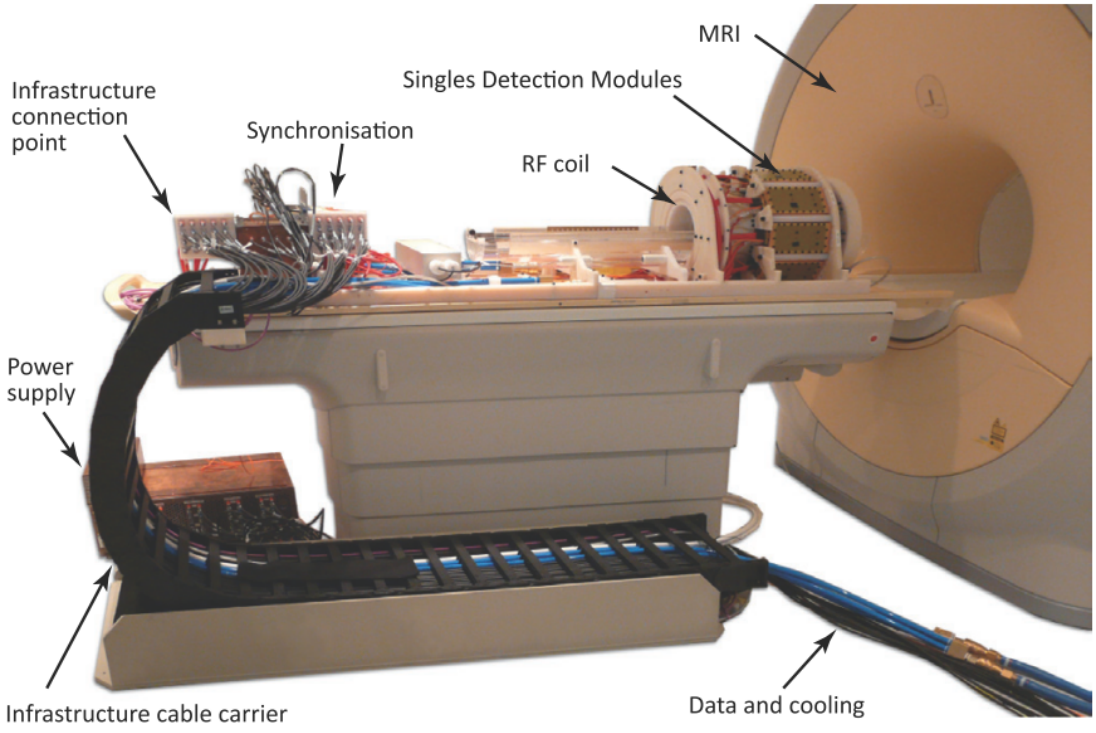


Figure 2.17: The PET insert mounted on a frame and placed on the MRI patient bed. Figure reprinted from [117]. © Institute of Physics and Engineering in Medicine. Reproduced by permission of IOP Publishing. All rights reserved.

Inside the PET gantry is located a non-removable dedicated MRI RF Tx/Rx volume coil (16-rod birdcage resonator, high-pass). It is surrounded by an RF shield (also known as an RF screen) in order to reduce potential mutual RF interferences between the SDMs and the RF coil. As the gamma radiation needs to pass through the coil components, the coil rods were designed as thin copper layers and electronic components were moved away from the PET FOV to reduce gamma attenuation. The coil is connected to externally-housed coil electronics as shown in fig. 2.18 and the combined PET/MRI FOV is 160 mm (transaxial) × 30 mm (axial) using one outer PET detector ring (95.6 mm with 3 PET detector rings).

The PET system was entirely designed from scratch and a lot of attention was given to the choice of non-magnetic materials and components as well as aspects for the electronics design to reduce RF interference in terms of both noise pick-up and RF field generation as much as possible. More details on the

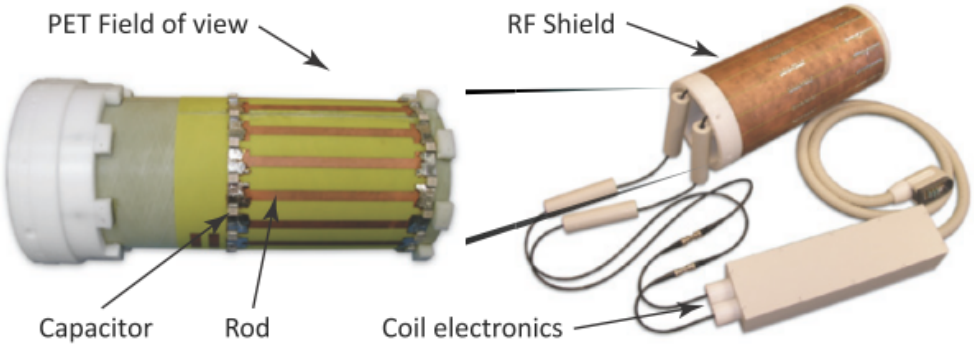


Figure 2.18: Dedicated MRI RF Tx/Rx coil: Left image shows the RF coil taken out from the RF shield. Right image shows the coil mounted into the holder with RF shielding and connected to the RF coil electronics box. The coil FOV is 160 mm (transaxial) × 160 mm (axial). Figure reprinted from [117]. © Institute of Physics and Engineering in Medicine. Reproduced by permission of IOP Publishing. All rights reserved.

MR compatibility aspects of the entire PET system can be found in [117].
The data acquisition platform for *Hyperion I* was also implemented from scratch and its architectural concepts were developed with the requirement to support the needs of future PET and PET/MRI systems with high numbers of photodetector channels. These concepts will be presented and discussed in detail in chapter 3. The topology of the acquisition system is shown in fig. 2.19.

2.5.3 Performance overview

A coincidence timing resolution measurement was presented in [115] by operating two SDMs with one-to-one coupling between scintillator crystals and SiPMs in an MRI. The result obtained was less than 530 ps which demonstrated the TOF-suitability of SiPMs in an PET/MRI environment.
The PET insert was so far populated with one detector ring, and a PET performance characterisation according to NEMA [34] specifications was presented in [144]. As this thesis deals with a data acquisition architecture design which was initiated with Hyperion I and implemented for it, the coincidence prompt, true, scatter, randoms and noise-equivalent count rates are shown as an excerpt from [144] in fig. 2.20. They were measured using a NEMA line source filled with *18*F in a rat-sized phantom. At an ^{18}F activity of approx. 30 MBq, the coincidence

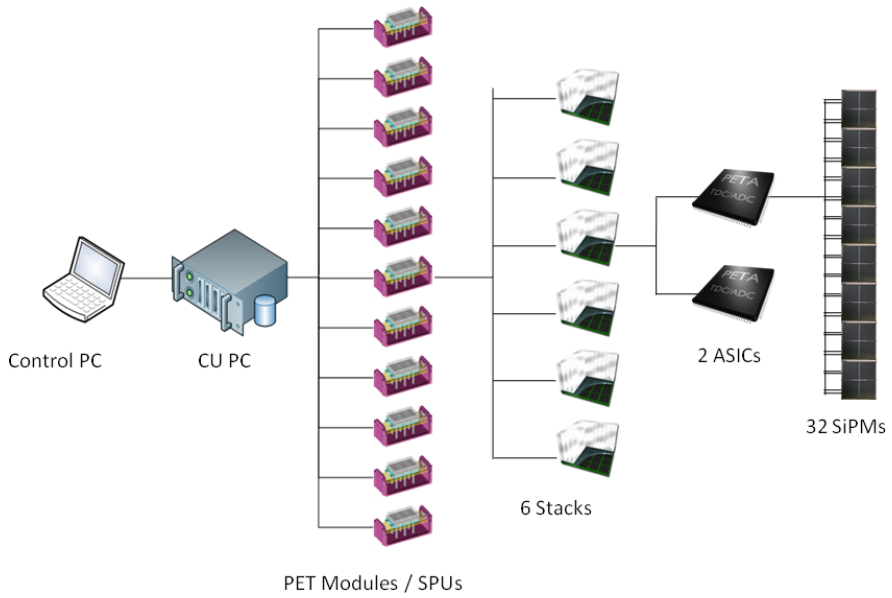


Figure 2.19: The data acquisition system is structured as a tree topology. (© 2012 IEEE. Reprinted, with permission, from [143]).

prompt rate is around 10 kcps. The peak NECR is approx. 7 kcps at an activity of 40 MBq. The courses of the different types of coincidence rates (trues, NEC, scatter and randoms) over the measured activity range are similar to the rates progressions shown in fig. 2.6 in the area indicated by "clinical range".

In [117], a detailed MR compatibility study was performed with Hyperion I, where different MR sequences were used to evaluate mutual interferences between the PET and MRI systems. During the application of EPI sequences, a small temperature increase in the SDMs resulted in an SiPM gain decrease and photo-peak shift of 0.5 %, leading to a coincidence rate drop of 2 %. The coincidence timing resolution of 2.5 ns and energy resolution remained unaffected by the EPI and the other gradient echo and turbo spin echo sequences. Regarding PET-related interferences, an MRI noise measurement revealed an average increase in noise of 21 % while the PET system acquired data from a point source. Performing MR imaging of a bottle phantom with six different sequences revealed an average SNR increase of 13 %. Finally, successful *in vivo* imaging was performed with a rat [117] and a mouse [144]. The rat was injected with FDG at an activity of 7 MBq to statically image the brain. The mouse was administered a dual-labelled PET/MR probe using ^{64}Cu with an activity of 20 MBq which accumulates in the

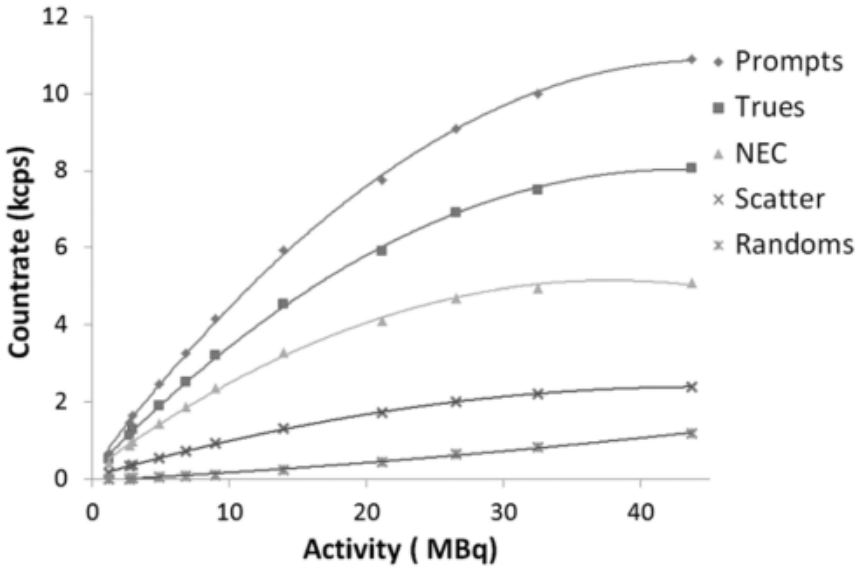


Figure 2.20: Coincidence count rate measurements of a line source in a rat-sized phantom done in accordance with NEMA specifications (© 2015 IEEE. Reprinted, with permission, from [144]).

liver and is visible on both PET and MRI. The distribution was acquired with dynamic PET and frame times between 10 s and 60 s.

2.6 PET insert *Hyperion II^D*

2.6.1 Introduction

The measurement results obtained with Hyperion I demonstrated that simultaneous PET/MR imaging with local PET signal digitization close to the SiPMs was possible despite the high number of digital electronics exposed to the hostile MRI environment. However, mutual interferences between PET and MRI were observed as mentioned in section 2.5.3. In addition to a raised MRI noise floor, MR image artefacts showing vertically dotted lines (known as *zipper* artefacts [145]) were observed which were caused by PET-electronics-related RF fields leaking out from the connections between the SDM housing and the shielded synchronisation cables. Moreover, the experiences gathered during *in vivo imaging* revealed the complicated setting up of the PET system for measurements, the inadequately large RF coil for mice imaging, and the lack of external trigger signal inputs for

PET image gating or MRI-synchronisation purposes. Therefore, in the second half of 2010, a follow-up project[3] began in order to develop a second-generation prototype with the aim of improving the PET/MRI performance obtained with Hyperion I and ameliorate the system setup and handling especially with regard to PET/MR *in vivo* studies. The new system referred to as *Hyperion II*^{D} was to be equipped with digital SiPMs from Philips (section 2.1.2.4) instead of an analogue-SiPM/ASIC combination to result in a fully digital PET signal data path and demonstrate the suitability of DPC sensors for PET/MR imaging. Satisfactory aspects of the Hyperion I system were kept for Hyperion II$^{\mathrm{D}}$ wherever sensible and adapted or improved, if necessary.

2.6.2 PET insert design overview

The structure of an Hyperion I SDM containing an SPU with up to six detector stacks in a 2 × 3 arrangement with point-to-point communication links between the stack and the SPU FPGA was kept for the SDMs of Hyperion II$^{\mathrm{D}}$. The SPU PCB underwent improvements to increase its MR compatibility and function [146] and the detector stacks were completely redesigned [147]. Figure 2.21(a) depicts an exploded view of the stack. The scintillation crystal array consists of 30 × 30 crystals with a length of 12 mm and a pitch of 1 mm × 1 mm suitable for high-resolution small-animal imaging. The array is optically coupled via a 2-mm-thick glass plate to the DPC sensors of type DPC 3200-22. The latter are mounted on the sensor tile in a 4 × 4 arrangement, yielding 64 SiPM pixels (sensor channels) spread over 16 sensor dies as shown in fig. 2.21(b) and (c). The number of SiPM pixels is thus the same as for a Hyperion I detector stack. As the signal digitization is performed sensor-internally, a separate board with ASICs was not required. The sensor tile is connected to the interface board equipped with a stack FPGA (Xilinx Spartan-6 LX45) and local bias voltage regulation for the DPC sensors.

[3]The works related to Hyperion II$^{\mathrm{D}}$ were co-funded by the German federal state North Rhine Westphalia (HighTech. NRW) and the European Union (European Regional Development Fund: Investing In Your Future) in the For SaTum project (Grant z0903ht014g); the Centre of Excellence in Medical Engineering funded by the Wellcome Trust and EPSRC under Grant WT 088641/Z/09/Z; and the EU FP7 project SUBLIMA, Grant agreement No 241711.

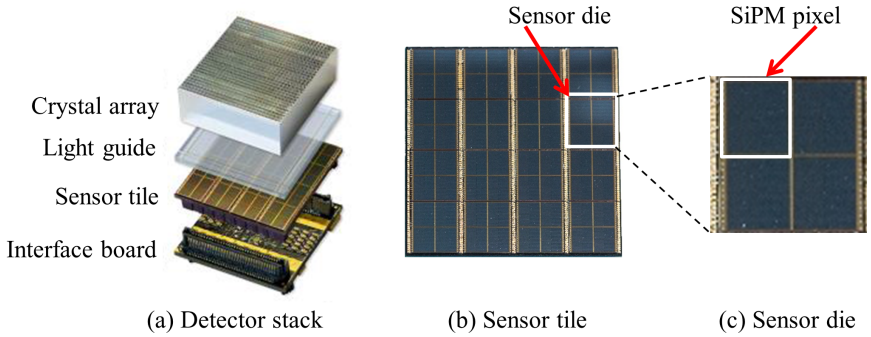


Figure 2.21: In (a) are shown the different components of a Hyperion IID detector stack. Picture (b) shows a sensor tile with 4 × 4 sensor dies. (c) visualizes one of the four SiPM pixels of a sensor die (Figure reprinted from [148]).

Figure 2.22 depicts an SDM with shielding removed. The electrical HDMI cable used for reference clock and synchronisation signal distribution was replaced by a single *plastic optical fibre* (POF) to decrease potential RF field leakage. The combined air and water cooling infrastructure was kept.

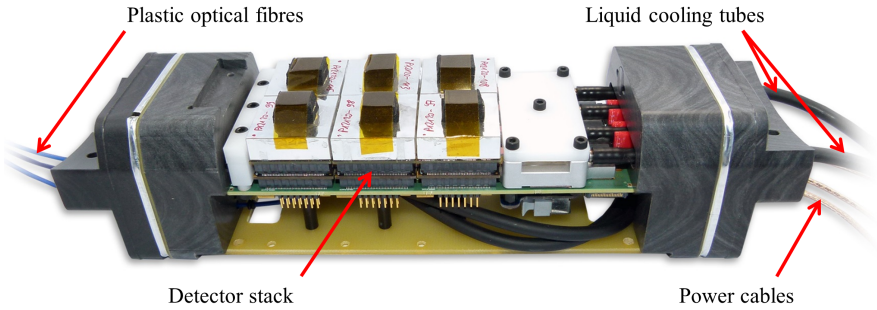


Figure 2.22: SDM with shielding removed and fully populated with six detector stacks (Figure reprinted from [148]).

The gantry of the PET insert is shown in fig. 2.23. It has similar dimensions compared to the Hyperion I gantry with respect to the PET FOV using ten concentrically mounted SDMs. The copper-coated housing was replaced by a carbon fibre shield to reduce eddy current generation, as it has good shielding characteristics at higher frequencies (RF range) and less conductivity properties for the frequency range used for MRI gradient coils [149]. When fully equipped with 60 detector stacks, the gantry offers a PET FOV with dimensions of 209.6 mm (tranxaxial) × 96.6 mm (axial) using 54000 crystals coupled to 960 DPC sensors corresponding to 3840 SiPMs.

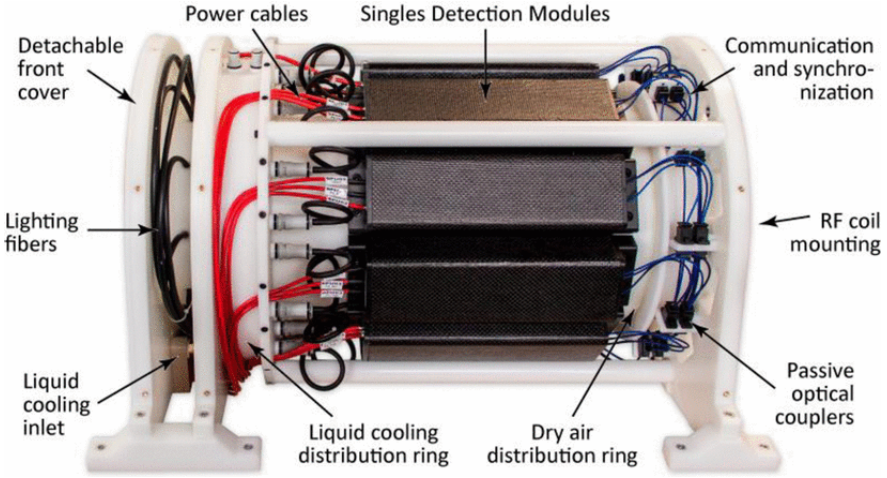


Figure 2.23: Hyperion II^D gantry: ten singles detection modules (SDM) are mounted concentrically and supplied with power, optical communication and synchronisation signals, water and air cooling. The dark carbon fibre shielding used for the SDMs is cleary seen. (© 2015 IEEE. Reprinted, with permission, from [125]).

In addition to the reference clock and synchronisation signal distribution, the synchronisation unit (shown in fig. 2.24 converts signals from plastic optical fibres to glass fibres commonly used in telecommunications. All signals between the insert and the data acquisition and processing server (DAPS) are transmitted via two multil-fibre cables which are connected via two Multiple-Fibre Push-On/Pull-off (MTP) connectors on each side. The replacement of 11 by 2 cables was done to ease the setup of the PET system. Furthermore, the synchronisation unit was equipped with external trigger in- and output ports to be used for synchronisation purposes by receiving ECG or respiratory triggers which are then inserted in the PET data stream. Additionally, a *remote trigger unit* (RTU) was designed to be located in the MRI technical room and to receive MRI trigger pulses to be forwarded to the synchronisation unit via a trigger input. This offers the possibility of direct synchronisation of the MRI with the PET system.

The gantry design was improved by allowing for removal of the MRI RF Tx/Rx coil. Three different coils with different MRI FOVs were made. An overview is given in fig. 2.25. The large coil is a 16-rung high pass birdcage resonator, the small coil 12-rod-birdcage resonator and the multi-nuclei coil is an inductively coupled surface coil. With each coil, the combined transaxial

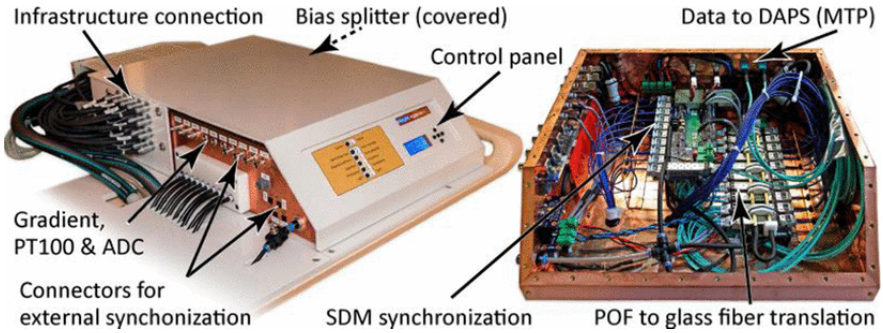


Figure 2.24: The central synchronisation unit of the insert: Left image shows the rows of external trigger in- and outputs for synchronisation and gating purposes. Right image shows the open unit revealing the optical fibre infrastructure with numerous fibres. (© 2015 IEEE. Reprinted, with permission, from [125]).

PET/MRI FOV is limited by the tranaxial coil FOV, whereas the axial PET/MRI FOV is always limited by the PET FOV.

Compared to Hyperion I, the gantry was design to be mounted on an MRI patient bed together with the synchronisation unit. The infrastructure (cabling, cooling tubes and power supply) is permanently attached to an MRI trolley with the bed on top of it. This greatly simplifies the transport of the insert to the MRI system. The insert placed in front of the MRI is shown in fig. 2.26. The infrastructure needs six connectors: Two for optical communication, two for water cooling, one for power and one to provide dry air.

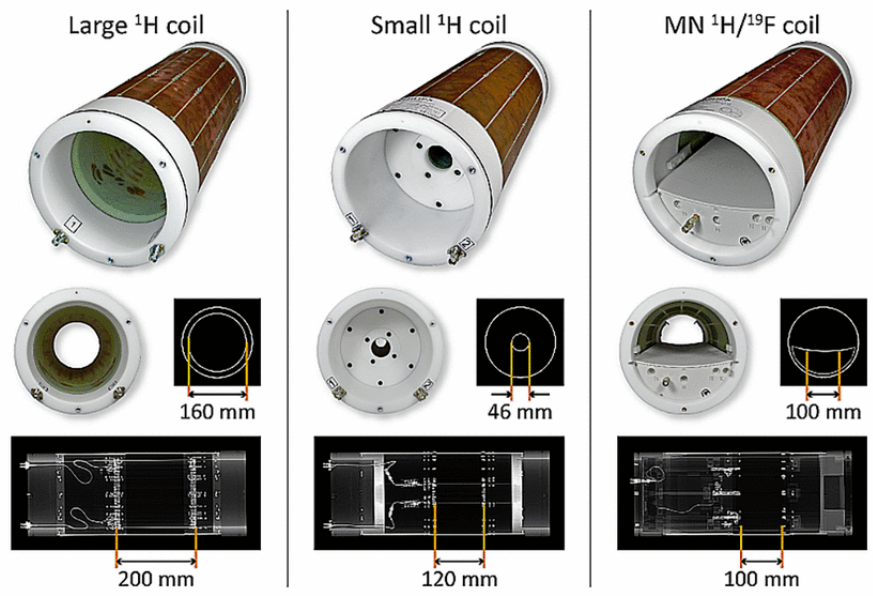


Figure 2.25: Overview of three available RF coils with reduced gamma attenuation characteristics. The large coil is suitable e.g. for rabbit and rat imaging, whereas the small coil was specifically designed for mice imaging. A multi-nuclei $^{19}F/^{1}H$ surface coil was designed for research using multiple contrast agents. (© 2015 IEEE. Reprinted, with permission, from [125]).

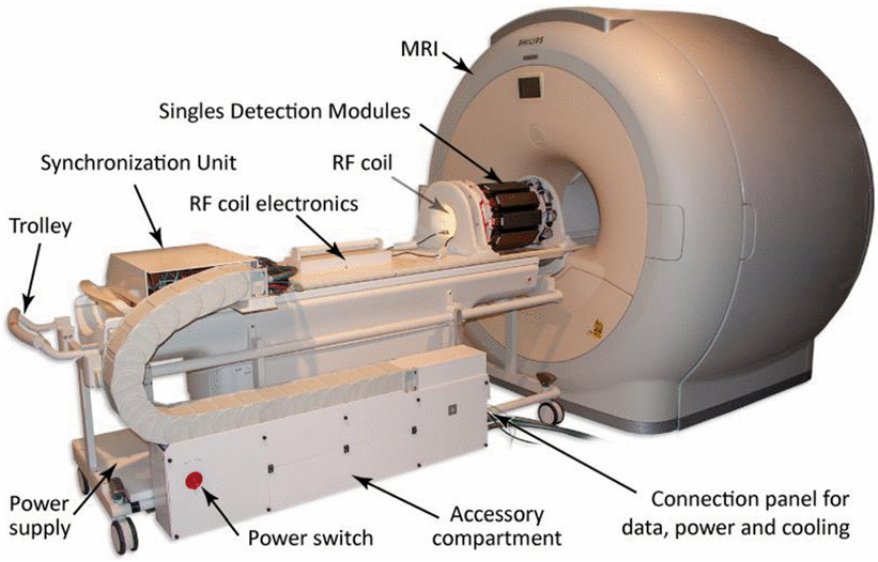


Figure 2.26: The insert placed on the patient table of the 3-T MRI. The cover of the PET gantry is removed, making the SDMs visible. (© 2015 IEEE. Reprinted, with permission, from [125]).

Chapter 3

An FPGA-based modular and scalable data acquisition architecture for PET and PET/MRI using silicon photo-multipliers

3.1 Introduction

The PET/RF insert Hyperion I (introduced in section 2.5) served as a research prototype for feasibility and research studies related to simultaneous PET/MR imaging [115] and as such was developed from scratch. The works related to research and development (R&D) of Hyperion I can be divided into four main fields:

- PET system geometry design based on GEANT4 simulations. Parameter adjustments and geometry definitions for the PET image reconstruction framework to be used with the PET insert
- Gamma-transparent MRI RF coil design and front-end detector development including scintillator, SiPM and mixed-signal ASIC designs

- MR compatibility of materials, components and PCB-design to enable PET/MR imaging with minimum mutual interference (see section 2.4.1)
- Concept and design of a communication platform for PET data and environmental sensor data acquisition

This chapter is concerned with the fourth of these areas. The communication platform has the main task of acquiring data from the PET detector front-end (ASIC and SiPM electronics in the case of Hyperion I). This data is gathered by the platform and forwarded to a data storage system. On the way, PET data is concentrated from many channels and may be stored as raw PET data as provided by the ASIC/SiPM combination (i.e. without further data processing) or may be processed to yield and store singles or coincidence data. At the time of the start of the HYPERImage project, PET acquisition platforms for commercial PET/CT systems were equipped with PMTs and often made use of analogue front-end electronics to process PMT signals in real-time [130, 150]. Any adaptations or improvements regarding signal processing techniques performed by analogue electronics require replacements of PCBs and components which is cumbersome and expensive. Furthermore, compared to their semiconductor-based counterparts, PMT-based detectors usually have a higher ratio of detection-area to number of signal channel outputs. Therefore, replacing PMTs by SiPMs in the case of e.g. clinical PET/MRI systems would lead to an increase of front-end PET data channels when compared to a PMT-based system with the same detector area dimensions. Processing PET front-end data at high rates while at the same time reducing the amount of inflexible analogue electronics can nowadays be achieved by using field-programmable gate arrays (FPGAs). As new generations of SiPMs have been undergoing continuous improvements in operating stability and performance, one of the central ideas during the conception phase of the communication platform was to develop concepts and requirements serving as cornerstones for a *data acquisition and control architecture* (DACA) adopting a one-fits-all approach. It may then serve for future preclinical and clinical SiPM-based PET systems in both the areas of PET/CT and PET/MR while fulfilling different PET parameter requirements depending on the application area.
The conceived DACA is referred to as the *HyperDAC platform* as it was first implemented for Hyperion I and the successful operation of which has been pre-

viously demonstrated and reported [151, 116, 152, 117]. The second-generation PET/RF insert Hyperion II^D, which was developed within follow-up projects (see section 2.6), also used the HyperDAC platform for control and acquisition purposes. It was additionally adapted and implemented with regard to the requirements described in section 3.2.2.
This chapter presents an overview of the general conceptual aspects of the DACA, introduces the communication-platform-related requirements of the Hyperion II^D insert and reveals how the DACA was specified and designed in order to meet these requirements. Architectural concepts of the DACA are outlined by covering the topics of the communication topology, modularity, scalability as well as communication protocol design. Moreover, aspects including platform versatility, robustness, hardware/software partitioning of the DACA, FPGA choices and MRI synchronisation possibilities in the case of the Hyperion PET insert requirements are presented. Afterwards, a short overview on the work-flows related to firmware implementation, simulation, synthesis and FPGA device mapping is given, followed by a presentation of the methods used to assess the DACA performance in terms of PET data throughput and transmission stability.

3.2 Methods

3.2.1 General architectural concepts of the DACA

The conceptual design of a DACA allowing high flexibility to fulfil the requirements of preclinical and clinical PET systems with different detector geometries and scintillator configurations needs careful attention regarding modularity- and scalability-related aspects. These aspects were addressed by allowing for flexible implementations of the DACA in order to cover a wide range of existing computing platforms and also allowing for exploration of alternative and novel ones. Such platforms need to address digital communication and data processing needs and are commonly divided into software-based computing platforms (computers, system-on-chips, embedded processors, DSPs), hardware-based ones such as ASICs and FPGAs (not using embedded processors) and FPGA-based hybrid implementations using processors plus dedicated hardware logic. The architectural concepts were designed with the above comprehensive aims in mind and are

presented in the following sections.

3.2.1.1 Communication network topology

The basic topological structure of the HyperDAC architecture consists of a tree topology as shown in fig. 3.1. Leaves of the tree represent data communication and processing nodes, or short: *nodes*. Node connections between adjacent tree levels are accomplished with point-to-point links. In the context of a detector data acquisition architecture, data from the detector front-end flows in the *downstream* direction towards data storage. Data flow from nodes at lower tree levels towards higher levels in the direction to the detectors (e.g. control data) occurs in *upstream* direction. Additionally, nodes of a same tree level may be interconnected to form a linear-mode-based daisy-chain (see section 2.1.4) to communicate between each other.

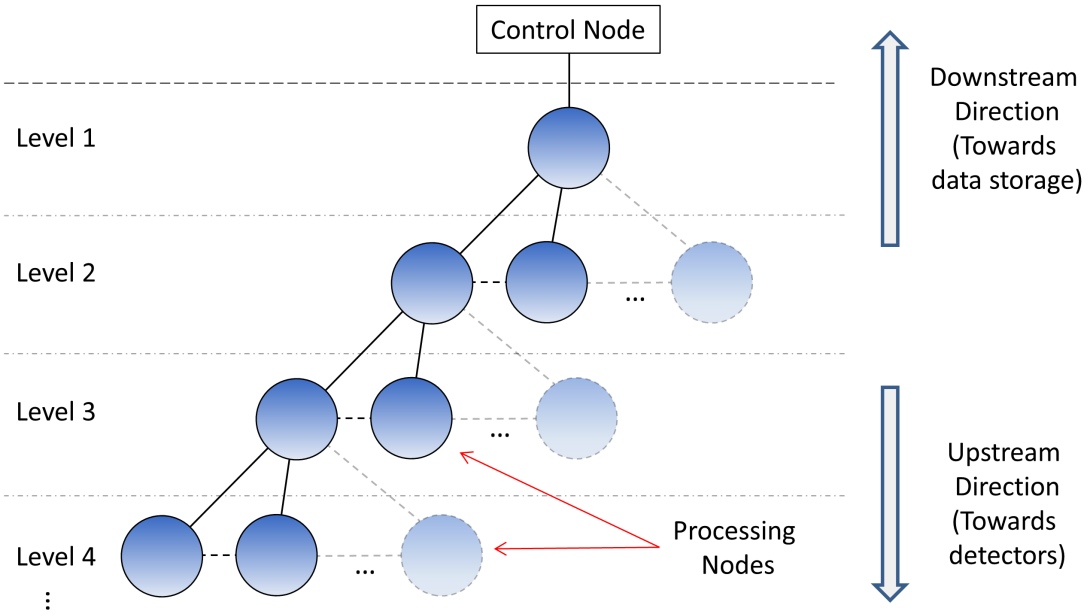


Figure 3.1: Generic HyperDAC architecture topology: Tree approach with optional daisy-chaining of nodes within a same tree level.

The node at lowest tree level is defined to control the nodes located at all other levels. Typically in the field of imaging systems, the person interacting with a system does this via a control console. Such a console can be an entity that is separated from the processing node at the lowest tree level as an alternative to

the level-1-node performing both the data acquisition and control. Therefore, a separate control node connected to the lowest node of the tree topology was added in fig. 3.1.
Communication between nodes is of bidirectional type and it is necessary to use separate physical communication channels for up- and downstream directions. In addition to simplified communication controls (no bus access arbitration required), this was considered important to avoid increased communication-latency variations and data traffic congestion particularly for cases of high detector data traffic in the downstream direction.
The daisy-chain communication option offers the possibility of distributed PET coincidence processing among nodes of e.g. tree level 2, instead of centralised coincidence processing approach at the lowest tree level (see section 2.1.3). Daisy-chaining between nodes of higher tree levels might be helpful for instance when using hit data of adjacent nodes resulting from scattered gamma events to increase the yield and accuracy of qualified singles during PET singles processing.

3.2.1.2 Communication protocol

All tree nodes (including the separate control node) communicate with each other using the dedicated *HyperDAC* protocol which was specified to suit the concepts and requirements of the DACA. Within the Open-Systems-Interconnection (OSI) protocol reference model [153, p.41-45], the HyperDAC protocol serves purposes which are comparable to those of the transport layer (layer 4). This means that it is used for end-to-end communication between nodes of the DACA, thereby being independent of physical-link types and their protocols located at OSI layers one to three. This ensures that the communication process via multiple nodes is defined by a single architecture-wide protocol and remains unaffected by changes or improvements with regard to underlying physical communication links.

Message data types

Data transmission between a sender and receiver is performed by grouping data (payload) with header information to form HyperDAC *messages*. Two different main types of message data were defined:

- Data originating from the PET detectors which can be for example detector

raw (hit) data, singles data or coincidences data. HyperDAC messages containing PET-detector related information are referred to as *PET data messages*.

- All other kind of data i.e. data related to the configuration and the controlling of the data acquisition system as well as status information. A message carrying such data is referred to as a *ctrl/status data message*.

Across the topological tree levels, ctrl/status messages occur in both the up- and downstream directions whereas PET data messages only appear in downstream direction. Daisy-chain connections are used for PET data message communication.

Message structure

The generic HyperDAC message protocol layout is depicted in fig. 3.2. The layout

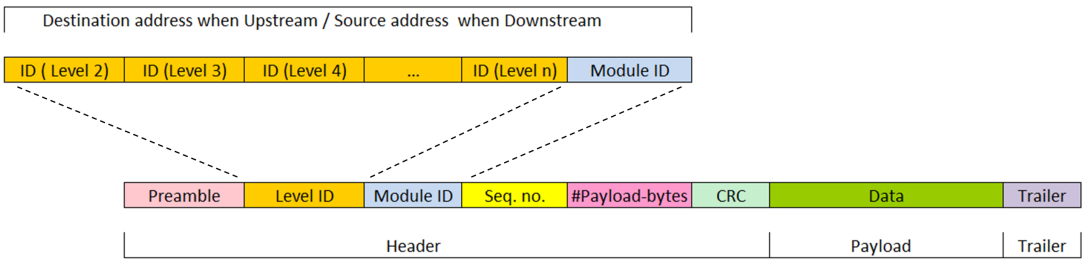


Figure 3.2: Overview of the HyperDAC message protocol structure conceived for the DACA-wide data communication.

is divided in header, payload and trailer fields. The message preamble serves as a delimiter to indicate a new message and contains a fixed bit pattern. The sequence number field ("Seq.no." in fig. 3.2) carries a number which is incremented with every newly generated message. Each entity that generates a new message increments its sequence number counter and inserts the new number into this header field. This field is used to identify missing messages originating from a same message source. The "#payload-byte" field contains the number of data bytes located as payload in the message. A further header field was added to allow for a cyclic redundancy check (CRC) of the header information in order to verify, if vital header information got corrupted during message transmission. Similarly, the message trailer may also contain a CRC value of the payload data

as an alternative to a fixed bit pattern to mark an end of the message.
Header fields carrying an identifier (ID) as denoted with "module ID" and "level ID" in fig. 3.2 are used to identify either the destination or the source of a message.

ID assignment definitions and message addressing scheme across tree levels

Within a node, an entity that is able to receive or send information via messages is referred to as a *module*. Each module is assigned a unique ID within a node. Modules are uniquely identified across a given topology with at least two nodes by assigning unique IDs to each node within every topological tree level. However, between different levels, node IDs do not need to be unique. The same applies to module IDs beyond the same node.
In the upstream direction, messages serve control or configuration purposes and modules receiving such messages can process their content without the need to know about the message source. The primary source of messages is considered to be the control node (level 0, or level 1 when integrated with data processing node), but not restricted to it.
In the downstream direction, a node receiving messages from a higher level either processes or forwards (bypasses) the message according to the node's local configuration solely by analysing the source address of a message. As the primary destination of messages in downstream direction is considered to be the single node at level 1 or 0, so that the vast majority of messages is forwarded to these nodes, a destination address within the message header in downstream direction is not required. In case downstream messages are destined for higher-level nodes than levels 0 and 1, this destination is identified via their source address using local decoders within nodes. When the control and PET data acquisition function are combined in a single unit, then the lowest node is node 1. If the acquisition and the control functionality are located in different units, then the PET data acquisition system (node 1) stores all PET data, but automatically forwards all ctrl/status data to the control node located at level 0.
The aforementioned conditions allow header space to be saved by omitting a source address field for messages in upstream direction and by omitting a destination address field for messages in downstream direction. Thus, depending on the transmission direction, the address field contains either the source or the

destination as denoted in fig. 3.2.
The domain used for ID assignment of modules and nodes is (ID $\in \mathbb{N}^+$). The number zero is used under the following conditions:

1. All modules that directly deal with PET data are assigned the module ID equal to zero. All other modules are assigned a number out of $\mathbb{N}^+$.

2. Within a tree with n levels, downstream messages that are generated at a level m with $m \in [2, n-1]$ have the value zero inserted in all level-ID fields of level range $[m+1, n-1]$

3. In the upstream direction, a message destination tree level m with $m \in [2, n-1]$ is identified by filling all message header-ID fields of levels $[m+1, n-1]$ with zeroes.

ID assignment definitions and message addressing scheme within a tree level

For the purpose of PET data processing performed at a same tree level (daisy-chain), only one level-ID field is used. This field contains information about the maximum distance between the source and the destination nodes in terms of node hops. The maximum distance is (n-1) nodes in case of n daisy-chained nodes. Incoming messages with a hop number greater than zero are forwarded by nodes via the daisy-chain with a decremented hop number in the ID field, if the message payload content does not match any user-defined conditions. Messages are discarded upon unmatched conditions and a hop number equal to zero.
As the addressing scheme for daisy-chain communication differs from the one in the down- and upstream directions, messages dedicated to tree-level-crossing communication cannot be used for daisy-chain data paths and vice versa.

Distributed ID information sources

If a node needs to send messages in the upstream direction to other modules of nodes at higher levels, then the message-generating module needs access to all node and module IDs of the destination modules. Typically, the control node will have to know the IDs of all nodes used within a DACA implementation which can receive messages from the control node. As messages might need to be forwarded by a node from a lower to a higher level (upstream), every node needs to be aware

of the node IDs of the nodes at the next higher level, it is connected with.
In the downstream direction, incoming messages to be forwarded by a node to a next lower level are modified with regard to their message header content by adding the ID of the node, the message came from into the corresponding level ID field. Thus, knowledge about node IDs at the next higher level is required. However, nodes and modules never need to know about their own ID.
Any node at a level $m < n$, which generates a new message to be sent downstream, needs to add level-ID fields of higher levels between $m + 1$ and n with values zero in the message header. To fulfil this requirement, all nodes need to be aware of the number of levels above their own level. This holds not only for ctrl/status data messages, but also for PET data messages. The latter may not only be created at the highest level (closest to the detector front-end), but also at lower levels. This occurs e.g. when PET raw data is transmitted to lower tree levels to be processed in order to yield singles or coincidences data. For such cases, PET raw data messages are not simply forwarded, but unpacked to process raw data from one or more messages yielding singles or coincidences data. Afterwards, the obtained data results are encoded according to the message protocol definitions and forwarded to lower levels which is considered equivalent to the generation of a new message with source address at a lower tree level.

Adaptive level-ID field length

While a message is forwarded from node to node in upstream direction, the ID fields used for levels that are left behind are of no use any more. Hence, before a node forwards a message, it removes its own level ID from the message header. This results in a shorter header length.
When a message is to be forwarded in downstream direction by a node, then the node ID field with the ID of the node from the next higher level is inserted into the header, which extends the message header length. Thus, during message forwarding across levels, IDs from nodes traversed by a message, are added, so that the message source address remains traceable at every tree level along the message path. The design of the adaptive level-ID field length of the header leads to an identical message header length of down- and upstream messages at a given tree level.

Message transmission examples

With the above set of definitions, message routing within the DAC is performed as visualised by the examples in figs. 3.3 and 3.4. In fig. 3.3, a message is sent from the lowest to the highest topology level and vice versa. As the destination and the source address is the highest level, the key identifier zero is not used for level ID encoding. Use of the later is demonstrated by two examples in fig. 3.4. In fig. 3.4(a), a message with destination node with ID 5 at level 2 is transmitted by the control node. A local decoder of the node in level 2 identifies a zero in the level ID field of the next higher level and thus delivers the payload to a local module instead of forwarding the message to a higher level. Figure 3.4(b) depicts a use-case where the number zero is added in level-ID fields for downstream transmission.

3.2.1.3 Scalability and modularity

Scalability in terms of a property for a data acquisition architecture describes the ability of being adjustable in order to satisfy the needs of requirements which may vary quantitatively as well as qualitatively. These adjustments should not alter the inherent architectural characteristics of the system.
Modularity describes the ability of an acquisition architecture of being composed from basic structures which allow for different configurations when detaching, mixing and reconnecting the basic structures with each other.
The higher the coherence of basic structures and the lower the interconnectivity required between these structures, the less effort is needed to expand or scale down an acquisition system. Consequently, modularity is an important aspect with respect to an architecture approach that has increased scalability capabilities. These properties are implemented within the HyperDAC architecture via the following characteristics:

- A tree topology with scalable size and optional daisy-chaining at every tree level.
- A modular addressing scheme of the communication protocol which automatically adapts to the topology size.

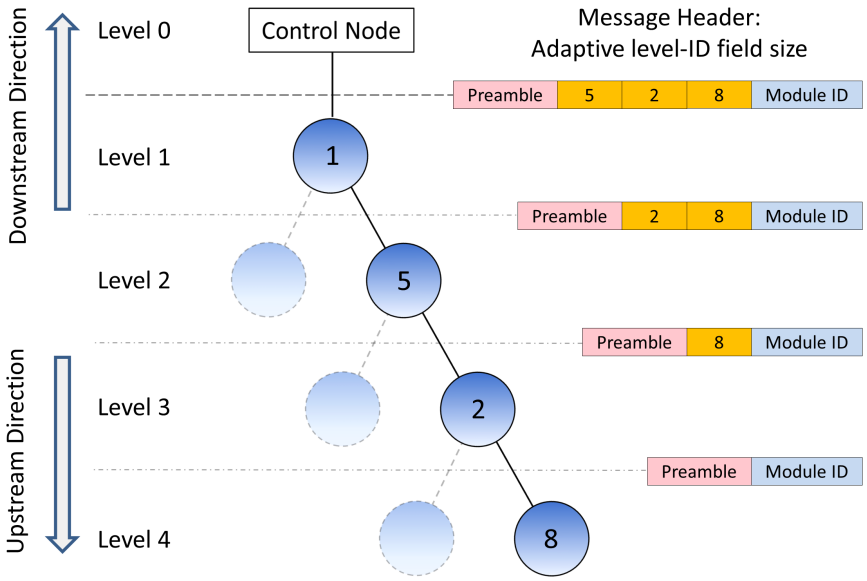


Figure 3.3: Example of adaptive level-ID field size for a message forwarded across all tree levels: In downstream direction, the level-ID fields are gradually removed towards higher levels. In the other direction, the level-ID fields are added by nodes while the message is forwarded towards the lowest topology level.

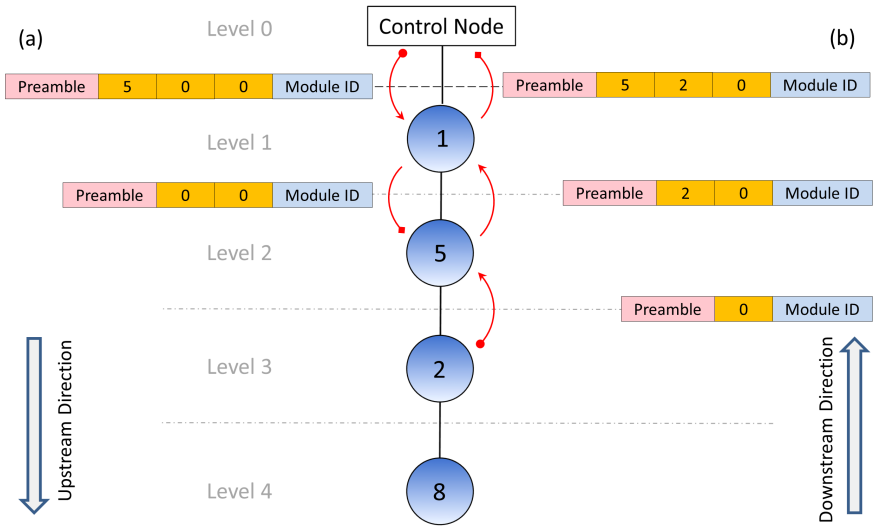


Figure 3.4: Examples of forwarding across a subset of tree levels: In case (a), a message is forwarded from level 0 to 2, in case (b), a message is forwarded from level 3 to 0.

- Modular design of message header decoders and encoders which allows for re-use between different node levels.
- Definition of node-level-independent commonly defined interfaces between modules and message address decoders/encoders. This enables module re-use and exchange at all topological node levels.

3.2.1.4 Further architecture characteristics

Hardware/Software partitioning

The above approaches are independent of the interconnection types between nodes. The latter may be implemented either in hardware or software nodes depending on the requirements. This allows for versatile possibilities to partition the acquisition architecture using different node types. These may also be exchanged with other types upon requirement adaptations later in time while the remaining parts of an implementation acquisition system remains untouched.

Generic node-internal data path structure

The generic structure of a DACA node is depicted in fig. 3.5.

Every node consists of a message decoder in the upstream data path and message type splitters, encoders and arbiters in the downstream direction. The decoder has the task of forwarding a message either to a node at next higher level or to forward payload data to node-internal modules. If needed, the latter can transmit ctrl/status data in downstream direction. As more than one module might wish to access the downstream data path, an arbiter is needed to grant data path access to requesting modules. Ctrl/status payload data is then encapsulated in a HyperDAC protocol header and trailer by the encoder which afterwards requests access to the downstream data path shared by ctrl/status as well as PET data messages.

Incoming messages from the shared data paths of nodes at the next higher level are split into different directions Ctrl/status messages are directed into the node-internal ctrl/status data path where they might either be directly forwarded to the arbiter/encoder unit or processed by local modules if a local ctrl/status data decoder is used. The message type splitters forward PET data messages to the node-internal PET data path. Here, data might either be processed or directly

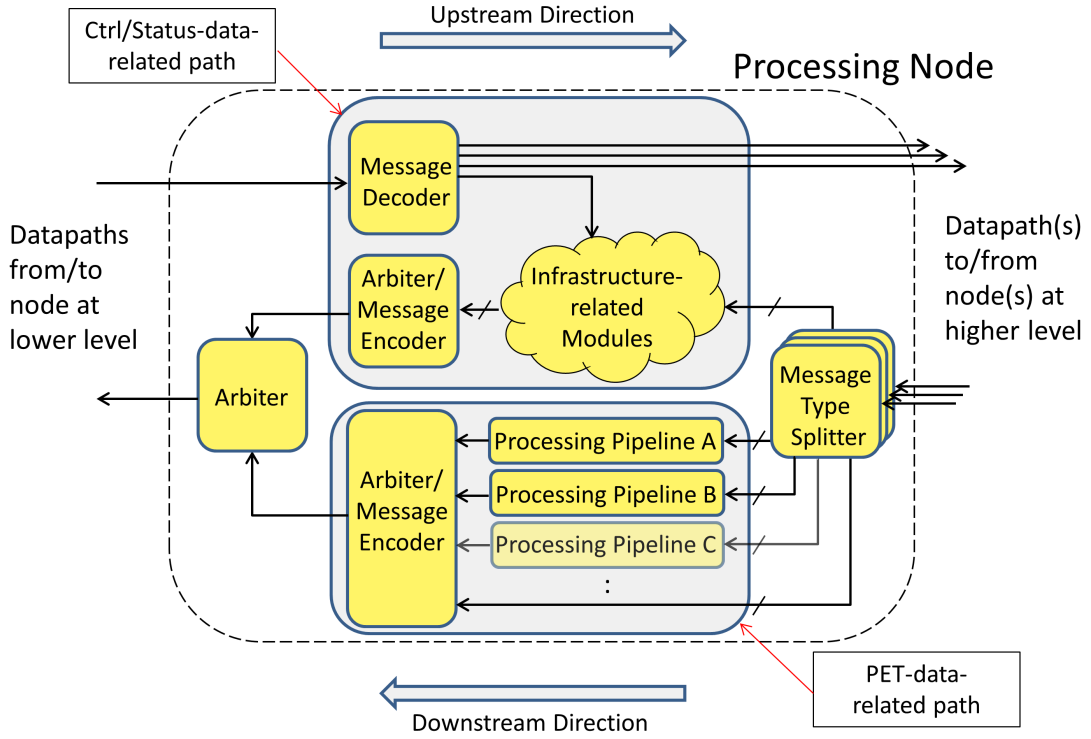


Figure 3.5: Generic structure of each DACA node: Message decoder, encoder and type splitter process message data according to protocol header information.

forwarded towards the arbiter/encoder unit of the PET data path. Depending on the local node configuration, a PET data message may be duplicated by the splitters and transmitted to a processing pipeline of choice as well as via a bypass path directly forwarded to the encoder. The message channel amount per splitter output type corresponds to the amount of higher-level nodes connected to this node. This maximises parallel data processing possibilities during data acquisition. All data messages from the PET data path competes with the ctrl/status data messages to access a shared logical interconnection to the node at next lower level.

Robustness and quality of service

HyperDAC message communication with the DACA is based on the store-and-forward principle [153, p.356]. Within nodes, message header decoders and encoders first analyse the coherence of the header information. Coherence means that the field content is verified with respect to valid value ranges. Upon suc-

cessful analysis, the complete message is forwarded and stored in a destination unit. If corrupted or invalid header information is identified, then the header including all following data is discarded upon detection of a new message header. Message integrity can be further increased by checking the payload data CRC check-sum or looking for a message trailer. In order to analyse the payload/trailer sections before forwarding it, a complete message first needs to be entirely stored prior to its integrity check and can only afterwards be either dismissed or processed/forwarded. These message integrity verifications are done in every node upon message reception in order to prevent unwanted behaviour originating from header or payload data corruption and thus improving the communication robustness of the DACA. In addition to message removal from the data paths upon detection of inconsistencies, these integrity checks also systematically allow the origin of inconsistencies to be verified, when appropriate reporting mechanisms are added within the DACA.

Before data is forwarded by a module, message decoder or encoder, sufficient space within the FIFO memory of the destination unit needs to be available to be able to completely store it. This is of particular importance for message decoders and encoders of a DACA node, as they receive and send messages from shared data paths. These paths should not suffer from data transmission blockage caused by a receiver and sender module due to local problems of any kind. Thus, message decoders and encoders need to be equipped with techniques that allow them to detect such blockages and take actions to release link access for other messages. To avoid imminent data loss when short data throughput peaks occur, data flow-control mechanisms along the data paths between tree levels (up- and downstream directions) need to be taken into account. Therefore, message transmitters should check, if the receiver FIFOs can store a complete message prior to sending it. If this is not possible, message congestion may be allowed up to message sources. This is acceptable for PET data, but should never occur for ctrl/status messages. Otherwise, if status messages cannot be successfully forwarded downstream towards the control node, the DACA may become uncontrollable and run into states unknown to the system user. As congestion might in first place occur in downstream direction when high PET data rates occur, prioritisation mechanisms between the two data types must be implemented. These ensure that ctrl/status messages will always be forwarded to the control node by

maintaining a fractional bandwidth for ctrl/status data. In the case that the acquisition system e.g. operates within its data throughput limitation, ctrl/status data is prioritised over PET data which results in loss of PET data.
When messages are sent between modules operating at similar operating cycle times (the time needed to process and forward a message), it is assumed that the destination module has sufficient resources to store incoming messages at arrival time. In case a ctrl/status message cannot be received (stored) by a destination module (in upstream direction), the control node needs be informed about a failed delivery. Based on this, further actions such as new transmission attempts or the possibility of investigating in the reason can be performed. However, destination modules may also require operating cycle times to process a message higher than those of the source module. Two reasons for this are 1) computational-intensive tasks which must be performed by the destination module or 2) communication with external peripheral devices operating at low speed. For such cases, message transmission flow control was defined. Message senders addressing destinations with aforementioned characteristics are provided with knowledge about the destinations' receive-FIFO depths. Here, flow-control-specific messages are used by senders in order to request an acknowledgement message from the destination module when its destination FIFO is empty or is below a certain threshold. Based on this information, a sender may determine the space available in the destination FIFO and derive the maximum amount of messages to be sent. This allows to avoid message rejection by message decoders due to a FIFO not able to store a complete message.
In downstream direction, a recipient may not successfully receive incoming messages due to consequences related to e.g. high communication workloads. Such message loss can be tracked by sequence numbers of successfully received messages being not successive. As an easier way to track a received message as an answer to a sent request, a message-ID may be included into the sender's message payload. In the destination module, this message ID is sent back to the sender with the requested data in a same message. If no message with the message-ID is received by the sender module within a defined time window, the message transmission can be repeated.
These principles offer flow control mechanisms while keeping the message transmission load as low as possible. This is of interest particularly in the downstream

direction in order to increase the share of available bandwidth for PET data messages while ensuring a robust ctrl/status message communication between source and destination modules.
When PET data acquisition is performed with the DACA (due to bandwidth limitation), PET messages may be discarded on an individual basis by nodes depending on congestion peaks along the topology branches. This may lead to reduced coincidence events when PET data is discarded in such ways that less coincident singles result. To avoid a randomly occurring PET message data rejection, the DACA should enter a gated acquisition mode. When one of the DACA nodes fulfil defined data path congestion criteria, a signal or ctrl/status message indicating that the node entered a "busy" state is transmitted to another node with synchronisation capabilities. The latter should as a consequence synchronously activate a periodically switching "gate" signal to all DACA nodes to activate and deactivate in defined time windows data acquisition at the detector front-end. This approach allows acquisition of PET data without the risk of randomly discarding messages during message propagation in the downstream direction, thereby maximising the coincident-events detection between gating-windows.

3.2.2 HyperDAC architecture implementation for Hyperion II^{D}

This section introduces the implementation of HyperDAC for the Hyperion II^{D} PET insert. The HyperDAC architecture implementation for the predecessor system Hyperion I served as a starting point and changes and adaptations to meet the requirements of Hyperion II^{D} were undertaken. An assessment of the throughput requirements was done for Hyperion I, based on which the FPGA-internal bandwidths and the interface throughput between the stack and the SPU FPGAs were determined. First, the throughput calculations are presented. Then, system requirements relevant to the acquisition platform are presented, followed by an overview of the implementation of the FPGA-based part of the acquisition architecture.

3.2.3 PET data throughput rate assessment

An initial assessment of the throughput requirements was done for Hyperion I and a gamma count rate calculation based on a tracer activity injection of 37 MBq (1 mCi) for PET imaging of rats served as the starting point. This activity value was determined as a tracer activity a bit higher than the typical activity range used for rats by a collaboration partner in HYPERImage. By calculating the gamma absorption rate within a scintillation crystal array, the number of hits and related hit data rates occurring between the digitization ASICs and the stack FPGA of a stack can be calculated. Similar to eq. (2.1), for a given point source activity N_0, the gamma radiation at a rate N_r striking a scintillation crystal array area A_{xa} which faces the PET FOV iso-centre at a distance r, can be approximated as follows:

$$N_r \;=\; \frac{A_{xa} 2 N_0}{4\pi r^2}\;\frac{1}{\text{second}} \tag{3.1}$$

As the gamma rate and not the decay rate are of interest, the factor 2 in the numerator of eq. (3.1) takes into account that one decay event gives rise to *two* annihilation photons propagating away from each other by approx. 180 °. With the gamma rate obtained by eq. (3.1), the mean number of gammas interacting with the scintillation material can be calculated as

$$N_{ab} \;=\; N_r(1 - e^{\frac{L_{xtal}}{\lambda_{LYSO}}})\;\frac{1}{\text{second}} \tag{3.2}$$

with the term in brackets representing the detection efficiency of the scintillator. It includes the crystal length in radial direction L_{xtal} and the material-specific LYSO absorption length λ_{LYSO}. For the radionuclide activity, $N_0 = 37\,\text{MBq}$ ideally assumed as a point source for eq. (3.1), a crystal array distance $r = 104\,\text{mm}$ from the iso-centre with an area $A_{xa} = 31.1^2\,\text{mm}^2$, a crystal length of $L_{xtal} = 10\,\text{mm}$ and an absorption length $\lambda_{LYSO} = 12.82\,\text{mm}$, the absorbed gamma rate equals $N_{ab} = 268\,\text{kcps}$. The ASIC data is read out synchronously to its coarse counter time window (referred to as a "time frame"). Therefore the following calculations are done per time frame of $52,43\,\mu\text{s}$. Then, the gamma rate equals 14 absorbed gammas per time frame. The average number of hits (triggered SiPM channels) generated per gamma interaction in a detector stack

was determined on a measurement setup and is between 3.5 and 5.5 hits per gamma interaction depending on the energy threshold settings of the ASIC and the radionuclide activity. Taking the average rate of 4.5, 63 triggered hits per sensor board occur during a time frame assuming an average hit distribution over the period of the time frame.
Further constraints to be taken into account are:

1. For each channel, the ASIC outputs 96 Bits of information which can be reduced to 40 Bits by removing unneeded Bit information during FPGA preprocessing.

2. The ASIC is read out by shifting out all bits from its internal shift registers, meaning that all 80 channels are read regardless of the number of triggered hits since the last ASIC read-out.

3. Gigabit Ethernet as a transmission standard between SDMs and the data acquisition server was chosen due to its wide-spread standard and maturity. This, however, introduces a throughput limitation of 1 Gbits/s (125 Mbytes/s) per SDM.

If all the six stack FPGAs of an SDM read and forward information from 80 channels (with 40 Bits each) per time frame, then 366.2 Mbits/s of unprocessed hit data are sent via the Gigabit Ethernet link excluding any other data overhead. Given the large margin between the estimated throughput data rate and the limitation of the gigabit link, the ASICs can be read out twice during one time frame. This would double the unprocessed hit data rate to 732.4 Mbit/s while still leaving sufficient margin for other control or status data until the 1-Gbits/s-limitation is reached. After each ASIC read-out procedure, all its channels are ready for new triggers from their SiPM channel counterparts. A gamma crystal interaction resulting in a group (or cluster) of triggered SiPM and thus ASIC channels (hits) as visualised in fig. 2.9 makes the triggered ASIC channels unavailable (blind) for new hits from subsequent gamma interactions until the ASIC is read out. During the time between two ASIC read-out procedures, a gamma interaction located in a crystal that is spatially close to a location of a cluster with triggered hits from an earlier interaction will lead to a so-called incomplete cluster. This is due to the used lightguide between the crystal array and the SiPM

array which allows to spread the scintillation light from a crystal to a group of SiPMs. Consequently, one SiPM can be triggered by light originating from different, spatially close crystals. ASIC channels triggered by SiPM signals from earlier gamma interactions cannot be retriggered from subsequent neighbouring gamma interactions until an ASIC read-out process takes place, which leads to incomplete hit clusters. This, in turn, may lead to a rejection of the detected hits due to criteria such as an incomplete cluster group or the total energy measured by the incomplete cluster being outside of the window of acceptance for a valid single (gamma interaction). If these criteria are fulfilled, an incomplete cluster may result in a mis-positioning of the gamma interaction origin during data processing when using e.g. centre-of-gravity-based algorithms such as Anger logic. Therefore, especially at high gamma count rates, a higher ASIC read-out rate reduces the possibility of obtaining incomplete hit clusters and thus increases the rate of detected singles as well as the singles' positioning accurary.
The data throughput estimation was done for the read-out and transmission of unprocessed hit data to the acquisition server which represents a worst-case in terms of data amounts to be transferred. This approach allows raw detector data to be gathered, which is of interest in the field of research, but which occurs at the expense of a lower count rate performance of the PET system. However, the limitation can be shifted due to an increase of ASIC read-out rate by processing hits locally in the SDM to obtain singles, thereby further reducing the amount of data to be transmitted via the optical link.
The data links between the stack FPGAs and the SPU FPGA were specified with 200MBits/s in order to be able to transmit the ASIC full shift register content of 96 Bits per channel once per time frame which leads to a throughput rate of 146.48 Mbit/s between a stack FPGA and the SPU FGPA.

3.2.3.1 Requirements

An overview of the characteristics related to the Hyperion II^D system architecture (i.e. detector and gantry geometries, mechanical and electrical infrastructure) was presented in section 2.6. Those affecting the DACA-related requirements will be pointed out in the following.

HyperDAC architecture topology

The Hyperion II^{D} PET system uses the same number of PET modules (called a Singles Detection Module (SDM)) and same number of detector stacks within each PET module as chosen for the proceeding system. An FPGA residing on each detector stack interacts with the detector front-end, i.e. the DPC sensors. In each SDM, an SPU FPGA located on the SPU board communicates with the stack FPGAs and data is forwarded by all SDMs to a central data acquisition and processing server where PET data is eventually stored. A control PC acts as the control node of the DACA and is connected to a data acquisition and processing server. The acquisition architecture topology used for Hyperion II^{D} with its topological hierarchy levels mapped to the processing nodes is shown in fig. 3.6. The implemented topology is a tree topology with three tree levels. Figure 3.7(a) depicts an SPU board with six interface boards each equipped with an FPGA. The geometrical arrangement of the FPGAs, which correspond to processing (tree) nodes, are assigned to the topology tree level mapping of fig. 3.6. As the stack FPGAs reside on the bottom side of the interface boards, a single and rotated interface board revealing the FPGA is shown in Figure 3.7(b).

dSiPM sensors

For the new PET insert, DPC sensors (see section 2.1.2.4) where chosen instead of a combination of analogue SiPMs read out by ASICs as used in Hyperion I. In addition to a new detector stack design required to provide an adequate power supply and cooling infrastructure for the dSiPMs, the FPGA-based HyperDAC architecture implemented for Hyperion I required design changes at the detector front-end to acquire data from the DPC sensors. These changes not only cover communication aspects in terms of hit data acquisition and sensor configuration, but also clocking, synchronisation and configuration of the sensors. These are the main tasks of the stack FPGA which was placed on the interface board (see detector stack in fig. 2.21).

A sensor tile is populated with 16 sensor dies which requires the stack FPGA to acquire hit data via 32 sensor data lines in total. The clock signal distribution which provides all DPC sensors of a tile with a clock signal was not realised with a dedicated clock fan-out chip as done on the SPU board. Due to interface board area constraints on the one hand and reduced flexibility with respect to clock sig-

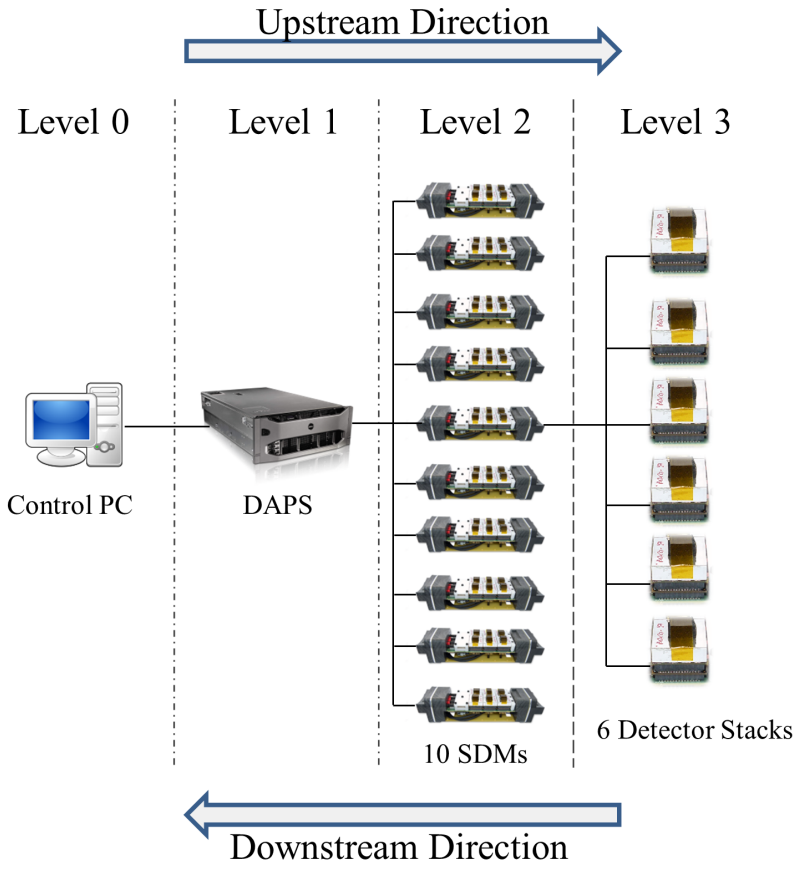


Figure 3.6: The topology of the HyperDAC architecture implemented for Hyperion II^{D} with its components mapped to topological tree levels. the computer acquiring data from the SDMs is referred to as the data acquisition and processing server (DAPS).

nal configurations when using a fan-out chip on the other, the clock distribution was instead performed by the stack FPGA. Furthermore, a bi-directional signal for synchronisation purposes was routed from each DPC sensor to the stack FPGA to allow for flexible control and trigger possibilities. The DPC sensors of a tile were connected via a serial joint test action group (JTAG) line in two groups of eight sensors in order to configure the sensor dies using JTAG. Thus, four JTAG traces were connected with the FPGA.
An overview of connections between components on the interface board and the sensor tile that are accessible by the stack FPGA are shown in fig. 3.8.

Environmental sensors, voltage regulation

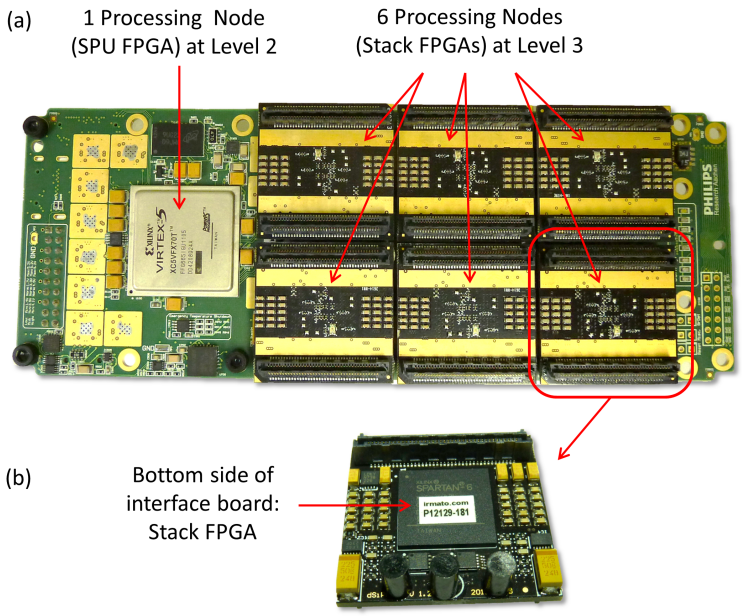


Figure 3.7: Figure (a) illustrates an SPU board with six interface boards and the mapping of its components to DACA tree nodes and tree levels. Figure (b) visualizes the Stack FPGA located at the bottom side of each of the six interface boards.

Encouraged by the useful information acquired via temperature, voltage/current, acceleration and gradient sensors for PET/MR research purposes with the Hyperion I system, these types of sensors where kept for the Hyperion II SDM design. A humidity sensor was added for Hyperion II in order to determine the dew point within an SDM and to avoid a temperature-rise of the fluid cooling above the dew point to avoid local condensation. The HyperDAC platform interacts with all environmental sensors to acquire sensor information. Additionally, all voltages are monitored and the sensor-die-related voltages VDDA and VBIAS are adjustable via the platform to select individual operating points of the DPC sensors.

FPGA components

The SPUs of Hyperion I were equipped with an FPGA of type Xilinx Virtex-5 FX70T. This FPGA offered at the time of choice one of the best performance-integration ratios. This model could still fit on the SPU PCB (27 mm x 27 mm) while offering highest amount of FPGA logic resources, memory and versatility of hard blocks compared to other Virtex-5 models [154]. The Hyperion II^{D} SPU uses

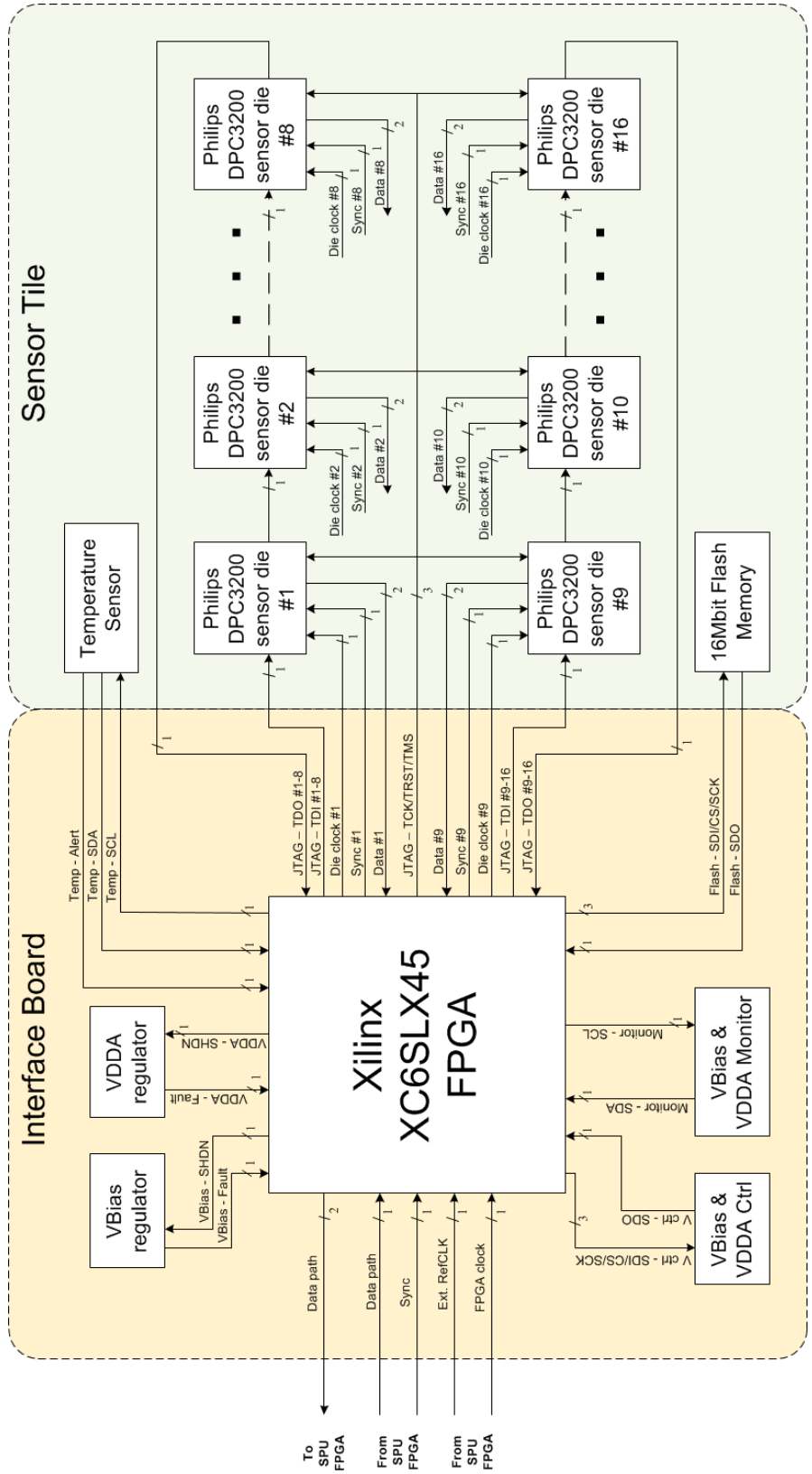


Figure 3.8: FPGA-external communication infrastructure of the interface board and the sensor tile.

the same type of FPGA. An upgrade to a next-generation Virtex-6 FPGA family with more resources was not done for the following two reasons: An FPGA with the same package was not available, meaning that a complete re-design of the SPU PCB would have been mandatory. Moreover, sufficient amounts of unused FPGA logic and memory resources were available in the Virtex-5 after mapping of the Hyperion I SPU firmware design, leaving enough room for additional firmware resources to be used for functionality added for the HyperDAC architecture implementation of Hyperion II^{D}.
The interface board of the new detector stack was equipped with an FPGA of type Xilinx Spartan-6 LX45. Similar to the criteria for the SPU FPGA, it offered the best performance-integration ratio out of the Spartan-6 family using a chip package covering an area of 15 mm x 15 mm to meet the interface board area constraints. The resources of the FX70T and the LX45 FPGAs are summarised in table 3.1.

Philips DPC firmware integration

The PDPC group has been developing firmware which configures the DPC sensor and acquires its hit data. This firmware operates on an FGPA made by Altera (Altera Corp, San Jose, CA, U.S.A.) which is used in PDPC products such as the PDPC Technology Evaluation Kit [155]. To accelerate the firmware development while using a validated firmware communication interface for the sensor dies, the goal here was therefore to achieve an efficient integration with the PDPC firmware at the detector front-end part of the HyperDAC architecture.
The PDPC firmware is divided into a control/configuration part and sensor data processing chain part with separated ctrl/status and hit data paths in the downstream direction. Communication with the firmware is performed by using the PDPC message protocol. A PDPC message decoder and encoder is located in the control/configuration part to make PDPC firmware units addressable by the protocol (referred to as modules in case of the HyperDAC platform). The control/configuration part is clocked at a different frequency to the data processing chain and makes use of the busy-wait polling approach as a communication technique [156, 157]. In this context, polling performed by a sender is used to verify if a destination is ready to receive data before transmitting a message. As this communication approach differs from the principles defined for the HyperDAC

Table 3.1: FPGA resource summary of the used models with focus on resources of interest for the HyperDAC platform.

	Part	Virtex-5 FX70T	Spartan-6 LX45
Logic Resources	Logic Cells	71680	43661
	CLB Flip-Flops	44800	54576
Memory Resources	Max. Distributed RAM (Kbits)	820	401
	BlockRAMs	148	116
	Total BlockRAM (Kbits)	5328	2088
Clock Resources	Digital Clock Manager,PLL	12,6	-,-
	Clock Management Tile	-	4
Hard IP Resources	DSP Slices	128	132
	PowerPC 440 Processor Blocks	1	-
	Ethernet Blocks	4	-
	RocketIO GTX Transceivers	16	-

platform, a bridge was required to translate the communication between the HyperDAC and the PDPC modules.

From the HyperDAC platform point-of-view, the configuration/control and the processing chain parts of the PDPC firmware are considered as two HyperDAC communication modules. The entire firmware as part of the HyperDAC design is referred to as the PDPC subsystem. Data communication with the control/configuration part of the PDPC firmware in both the up- and downstream directions takes place via a serial data path. The PDPC processing chain outputs data via a two-bit-wide data path in the downstream direction. As data communication with the PDPC subsystem is performed using the PDPC message protocol, all data to be sent as payload in upstream direction addressing the PDPC subsystem is encapsulated in a PDPC message. With the subsystem integrated into the HyperDAC design, the PDPC message additionally needs to be wrapped in a HyperDAC message. This allows PDPC-firmware related messages

to be sent e.g. from the control-PC via HyperDAC architecture nodes to the destination node using the PDPC subsystem as one of its HyperDAC modules. The same applies to the downstream direction path where PDPC messages leaving the subsystem are wrapped in a HyperDAC protocol by the protocol wrapper before being forwarded.

Node communication interfaces and data bandwidths

Data transmission between the data acquisition server and the PET modules of the Hyperion I system was performed using UDP/IP over optical Gigabit Ethernet. This offers a large bandwidth per PET module using a standardised and widespread communication interface supported by numerous manufacturers of computers and embedded systems. UDP was favoured over TCP because of a resulting simpler and smaller FPGA design and the possibility to transmit data as streams with the highest Gigabit Ethernet bandwidth usage. In case of ctrl/status data, flow control and fault detection are handled explicitly by the HyperDAC protocol whenever needed. The GbitE/UDP/IP interface was kept for communication with the SDMs of Hyperion II^D.

The data interface between the SPU and stack FPGAs provides a bandwidth of 200 Mbit/s in the downstream and 100 Mbit/s in the upstream direction. The downstream bandwidth matches with the one specified for the PDPC firmware. When the RAW-data mode of the PDP processing chain is selected (i.e. acquired hit data is forwarded without any data corrections), a maximum of 32 DPC sensor data messages per sensor die plus a framing message per sensor die can be acquired by the chain within a time frame of 327.68 μs. When the chain operates in RAW-data mode, 14 bytes are used to store information of a sensor message. This leads to a total of 32 sensor data messages $*16$ sensors $= 512$ sensor data messages plus 16 framing messages per time frame. As the chain stores data consecutively in internal memory, the first 32 data messages acquired from each sensor die during a time frame are stored and subsequent messages are ignored until the end of the time frame. With the additional framing message storage per frame, the total number of sensors messages equals 33. If all 16 sensor dies of a sensor tile transmit 32 data messages, the following maximum HyperDAC PET

data message is obtained:

$$
\begin{aligned}
&9\,bytes \text{ HyperDAC message header}\\
+&5\,bytes \text{ HyperDAC-message-specific payload}\\
+&5\,bytes \text{ PDPC message header}\\
+&4\,bytes \text{ PDPC-message-specific payload}\\
+&14\,bytes \times 16 \text{ framing messages}\\
+&14\,bytes \text{ message data (RAW mode)} \times 16 \text{ sensor dies} \times 32 \text{ sensor data messages}\\
=&7415\,bytes
\end{aligned}
\tag{3.3}
$$

Thus, the transmission of the maximum message size per time frame leads for each stack to the maximum PET data rate of:

$$\frac{7415 bytes}{327.68 \mu s} = 180,688\, Mbit/s \tag{3.4}$$

This data rate for PET data messages is reached in the downstream direction taking into account the PDPC and the HyperDAC message header overheads. With a communication interface bandwidth of 200 Mbit/s, this leaves sufficient bandwidth for ctrl/status messages e.g. to report SiPM temperature sensor information during PET measurements.

However, six stacks delivering the aforementioned peak PET data rate leads to a sustained aggregate of 1084.13 Mbits/s which is above the theoretical bandwidth limitation of Gigabit Ethernet. Therefore, provided that the SPU FPGA forwards all incoming PET data messages, the SPU-FPGA data path becomes the bottleneck within the FPGA-based part of the acquisition architecture when the PET detector is operated at count rates high enough to saturate the data processing chains of the stack FPGAs. An overview of the SPU board components and signals accessible by the SPU FPGA are drawn in fig. 3.9.

Synchronisation, clocking, time stamping, external triggering

All SDMs are provided with a clock signal from a single clock source. This signal is used to drive all time stampers of the acquisition platform synchronously to time-stamp PET data. This makes it possible to identify coincident Singles

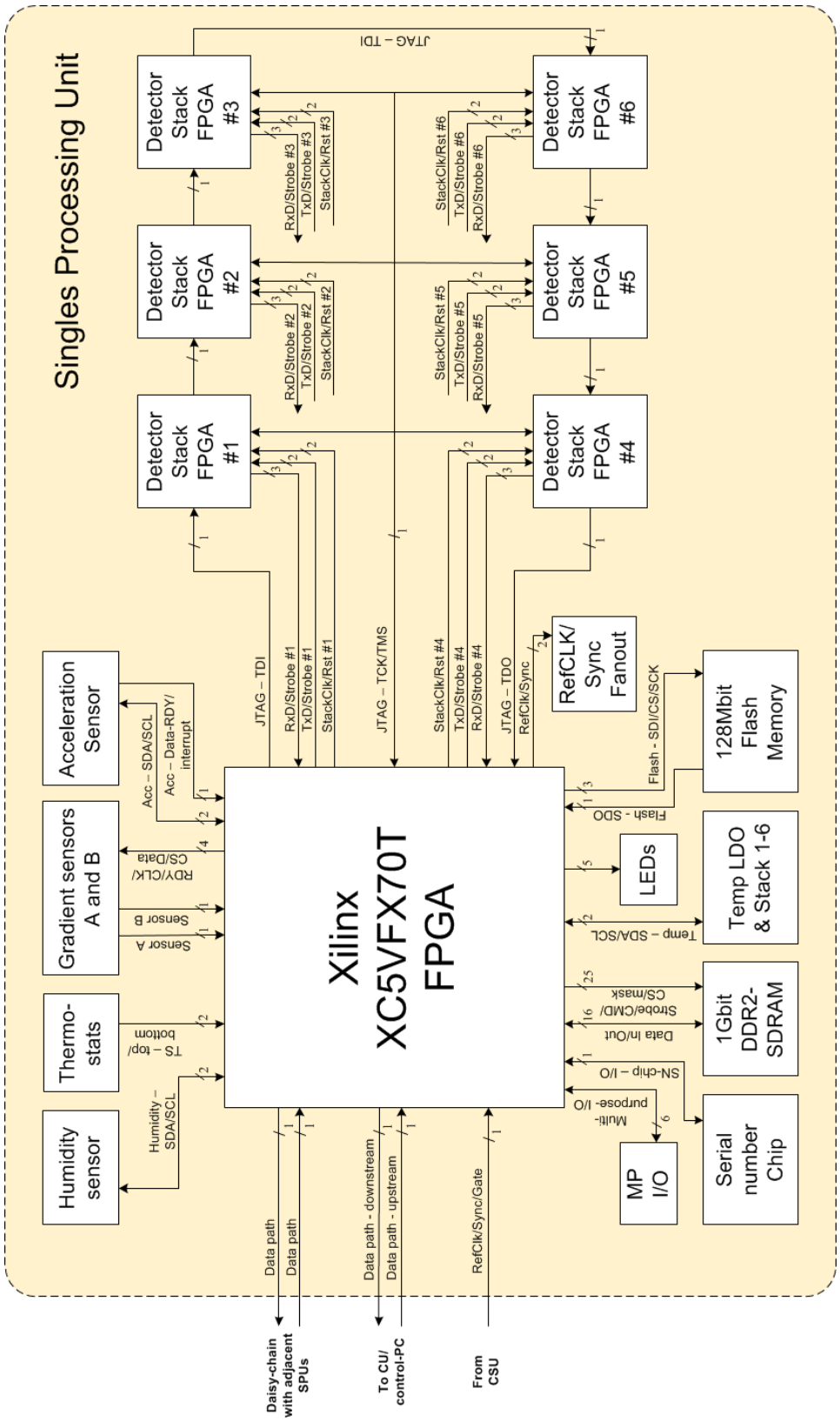


Figure 3.9: SPU-FPGA-external communication infrastructure of the Singles Processing Unit

with respect to the time at which they were detected. The distribution of this clock signal within the PET system is depicted in fig. 3.10. The PET-system-wide reference clock referred to as "refCLK" is generated and distributed to all SDMs by the clock synchronisation unit (CSU). The CSU itself is based on an SPU board with an adapted FPGA firmware design and special daughter-boards connected to the connectors normally used for the Stacks in the SDMs. The refClk is generated by a 100 MHz oscillator and either fed through the CSU-FPGA or directly to a fan-out chip. The latter distributes the refCLK signal with low jitter to the SPU FPGAs of the SDMs. From there on, the refCLK is forwarded via local fan-out chips to all Stacks of the SDMs. Each stack FPGA, in turn, distributes the clock signal to each sensor die of the sensor tile. As the refCLK signal is routed through FPGAs, FPGA-internal clock synthesis and phase shifting can be applied to the clock signal on its way towards the stacks. For Hyperion II^{D}, the copper-HDMI-cable that was used for signal transmission of the refCLK and global synchronisation-related signals was replaced by a single optical fibre. Hence, signal encoding was required to combine the clock signal with other signals to be applied globally to all SDMs such as synchronisation and gating signals. The latter two are used to synchronously start and stop the PET data acquisition or to optionally gate (interrupt) the acquisition for defined time windows when the system operates in bandwidth limitation as introduced at the end of section 3.2.1.2.

The refCLK signal not only synchronously clocks the sensor dies as shown in fig. 3.10, but also needs to drive counters in each FPGA that are used for time stamping purposes of PET and ctrl/status data. This approach was implemented for Hyperion I and was taken over for Hyperion II^{D}. As described in section 2.1.2.4, the DPC-sensor uses an inverter chain as a fine counter and a coarse counter covering the time range of the fine counter to time-stamp successfully validated Hits. Operated at half the sensor die clock frequency of 200 MHz (i.e. double the clock period equalling 10 ns) with a width of 15 bits, the coarse counter covers a time frame of $2^{15} * 10\,\text{ns} = 327.68\,\mu\text{s}$. To extend the time stamp range, the DPC sensors' coarse-counter overflows are counted by the DACA using *frame counters*. The latter are 32-bit-bide and thus cover a time range of approx. 16 days being more than enough for nuclear imaging purposes. Similarly to Hyperion I, PET data was to be time-stamped over the whole range of frame, coarse

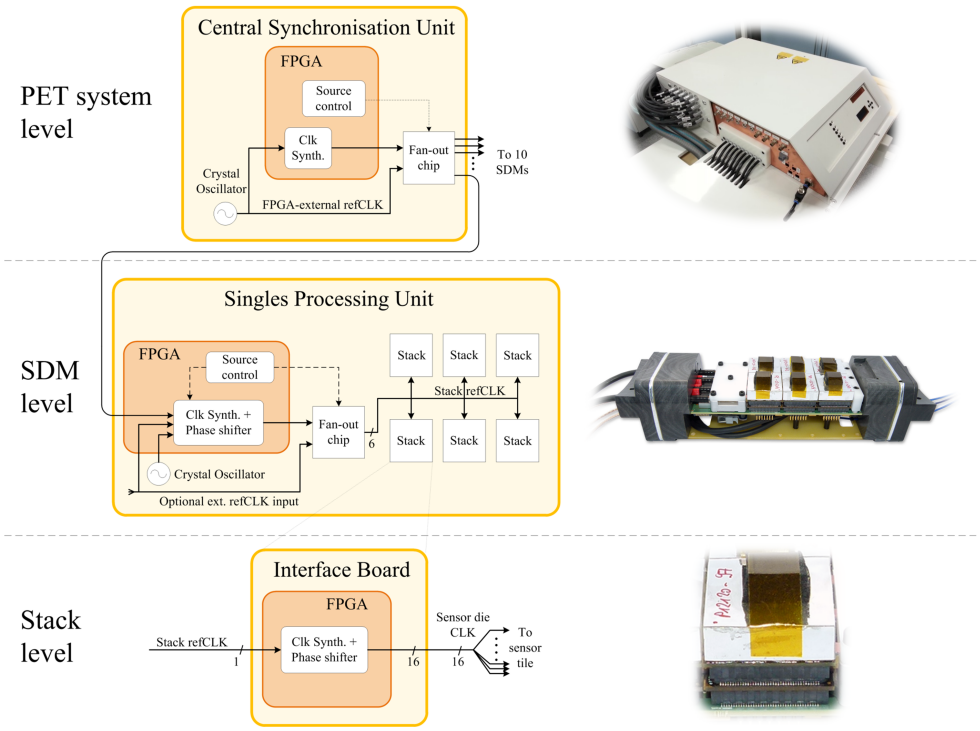


Figure 3.10: Clocking infrastructure of the PET insert visualised for the reference clock (refCLK) and refCLK-derived clocks at PET system, SDM and stack level. Arrows with dashed lines indicate clocking-related control signals, arrows with full lines indicate clock signal paths. At SDM level, the number of individual stack refCLK signal lines on the SPU is indicated by the number Six below the signal line close to the fan-out chip. Frequency and phase of the clock signals can be modified in each FPGA via integrated clock synthesizer and phase shifter blocks (Figure reprinted from [148]).

and fine counters, whereas the time stamp granularity for ctrl/status data was set to units of time frames, i.e. frame counter step size. A time frame in the context of the PET time stamping is synonymous to the full coarse counter sweep, i.e. a coarse counter overflow.
The CSU of the new PET system was enhanced by adding optional trigger input and output channels. Detected input triggers are to be time-stamped and the trigger channel and its time stamp to be forwarded as ctrl/status data via the CSU downstream data path and eventually processed and stored in the DAPS.Output trigger channels can be configured by the control node to create periodic triggers which may be configured to trigger upon a configurable input trigger conditions.

Time-frame-based PDPC message transmission

The PDPC subsystem stores, processes and forwards acquired DPC sensor data on time frame basis. This means that all DPC sensor data acquired and processed during one time frame is encapsulated in a single PDPC message which is then transmitted in downstream direction. The PDPC message length varies depending on how many DPC sensor messages were acquired by the processing chain per time frame. At the beginning of a new time frame, all DPC sensor data from last time frame is forwarded and therefore needs to be wrapped in a HyperDAC PET data message to be sent in downstream direction.

Flash Memory for FPGA design and DPC sensor information storage

Each SPU was equipped with a 128Mbit-large Flash memory to enable an SPU-FPGA configuration after applying power to the SDM. In case of a corrupted FPGA bit-stream image, the SPU FPGA cannot load the configuration successfully, leading to a situation where no communication is possible to reprogram the Flash memory. This would make it necessary to remove the SDM from the gantry and to open the SDM in order to reprogram the memory or the FPGA via a dedicated JTAG connector. To avoid this situation, a multi-boot feature of the Virtex-5 was used, allowing the FPGA to load a second fall-back (golden) image, in the case that the main bit-stream image load fails. With two bit-streams occupying less than half of the Flash memory space, enough space is available for e.g. Lookup-table-content to be loaded after FPGA configuration into FPGA-

internal BlockRAM for PET-data-processing-chain-related information.
Similarly to the SPU board, every sensor tile was also equipped with a Flash memory. It can be used not only to store inhibit-bit information for the sensor dies to be loaded by the stack FPGA. The FPGA itself may load a bit-stream for its own configuration after power-up.

DDR2-SDRAM

The SPU board houses a large 128MB DDR2-SDRAM chip which is accessible by the SPU FPGA. The memory may be used as a larger buffer to temporarily store PET data before, during or after data processing. DDR2-SDRAM is optimised for burst-oriented data access, meaning that consecutive write or read operations at consecutive memory addresses allow operations at a high bandwidth. When alternating read-write accesses are performed, this memory type suffers from lower average bandwidths due to increases in memory access latencies. As FPGA-internal memory is of type static RAM, the external SDRAM chip on the SPU is meant to be complementary with respect to memory access behaviour, but with a large capacity compared to the internal memory.

3.2.3.2 Implementation

HyperDAC message processing and arbitration

The message-processing units as shown in fig. 3.5 were implemented for the Stack, SPU and CSU FPGA designs. Message header decoders and encoders as well as arbiters are used in all FPGA designs of the acquisition platform, whereas the message type splitters are only needed for the SPU FPGA design.
The message header decoder used for the upstream data path parses the entire header of a message and verifies its integrity prior to any data forwarding. The verification steps cover valid preamble detection, valid destination-ID ranges and calculation and comparison of the header-CRC information. Moreover, the decoder verifies if the recipient identified within the header is ready to accept a new message. The recipient is either a node-internal module or in case of message forwarding to a node at a higher topology-tree level a data transmission interface like the one between the SPU and the stack FPGAs. A message forwarding attempt is repeated three times with a defined time window and aborted when a

recipient is not able to receive a message. A failed forwarding attempt is reported via an Error Handling Unit (EHU) back to the control PC together with header information of the undelivered message. The latter is discarded from the input queue by the decoder to allow the forwarding of other messages. This avoids any blockage of the data flow resulting from a destination module incapable of receiving new data.

In the downstream direction, the message encoder used to encapsulate payload from node-internal modules or to forward messages from a next higher tree level was designed to yield the highest throughput while being robust against message congestion and unexpected message transmission behaviour. Since multiple data sources (node-internal modules or FPGA-external data from other nodes) want to access the downstream data path, high attention was given to in making possible to transfer data with very low latency in order to use efficiently the available downstream data path bandwidth. The message encoder is capable of forwarding data with an updated or a newly generated header at one data word per clock cycle. This, in turn, requires that data from FPGA-internal modules or downstream paths providing data from the next higher tree level is made accessible to the encoder input with the same throughput. Therefore, units providing data to the encoder are specified to do so by using e.g. intermediate FIFOs. Failing in providing data to be read continuously by the encoder to be forwarded results in an exclusion from the access to the encoder, as this is considered as an unexpected blockage behaviour. This releases the access to the downstream data path for other units, thereby ensuring robustness against blockage due to inconsistent message transfer behaviour from a possibly malfunctioning sender. The encoder also checks for structural message inconsistencies of messages originating from other nodes and only forwards these in case of a successful verification.

As previously mentioned, the downstream data path is shared by multiple ctrl/status- and PET-data-sending modules. They may wish to transmit data at a similar time and therefore compete for the data path access. Thus, the access needs to be controlled by an arbiter. When a module requests access to the data path, it has to wait until the access is granted by the arbitration logic. The arbitration algorithm is based on a packet-to-packet (packet-based) round-robin scheduler [153, p.412]. All requesters are treated with same priority at packet-level, meaning that every module gets the possibility to transmit data of

one complete message within one round-robin cycle (i.e. each of the connected modules gets the chance to access the data path, if it requests it). To increase the fairness, only modules with requests raised at the beginning of a cycle will get access granted. While the arbiter addresses the requests from participants available at cycle start, any new incoming requests from other participants will be ignored and addressed at the next round-robin cycle. As an example, if three modules A,B and C form a round-robin cycle and A and C request data path access at arbitration cycle, the aforementioned increased fairness avoids e.g. with module A accessing the path due to a given grant, module B suddenly requests access and obtains before module C, although the latter requested access before B.

Arbitration and message header encoding towards the shared downstream data path are performed in parallel using two branches with the arbitration process divided in two stages as shown in fig. 3.5: An encoder entity and an arbiter (first stage) are assigned for each data message type. Arbitration is performed between all requesters of a same message data type (i.e. ctrl/status or PET data). It follows that the second arbitration stage for messages from the two data branches allows message forwarding between the two message types to be prioritised in different ways, if needed. Requesters with data from higher tree levels and requesters with node-internal data are treated equally.

FPGA-internal data path widths and clock domains

In all FPGA designs, 8-bit-wide data paths are used for ctrl/status as well as shared ctrl/status/PET data transport. With the frequency ranges supported by the clock infrastructure and the configurable logic blocks of the Virtex-5 and Spartan-6 FPGAs, data transmissions of the order of gigabytes per second are achievable. This supports communication transmission speeds used by off-the-shelf computer network adapters offering data rates of $1, 2$ or $4\,\mathrm{Gbit/s}$ for for computer systems such as the DAPS and the gigabit transceivers of the Virtex-5 FPGA.

The Hyperion II^{D} FPGA designs each comprise several clock domains for flexibility as well as bandwidth adaptations. The logic linked to ctrl/status and shared ctrl/status/PET data paths is clocked with $100\,\mathrm{MHz}$ and forms the system clock domain which results in data path bandwidths of $800\,\mathrm{Mb/s}$ or $100\,\mathrm{MB/s}$. An

ethernet block (hard IP) of the Virtex-5 FPGA, which is used for the GbitE interface, is clocked at 125 MHz and is equipped with an 8-bit-wide data path on the FPGA-fabric side to yield the specified data bandwidth of 125 MB/s.
Data communication between the Stack and SPU FPGAs is performed with an interface which operates at a frequency of 100 MHz. Although the frequency is the same as the system clock frequency, it was separated from the system clock so that a frequency modification or complete interface design replacement is possible without directly affecting the performance and design mapping properties of the logic in the system clock domain due to a frequency change. The ctrl/status-related part of the PDPC subsystem is driven by the system clock and thus share the same clock domain with the ctrl/status-related units of HyperDAC. However, the clock for the PET data processing chain as a part of the PDPC subsystem needs to be synchronised with the sensor die clock signal. This is mandatory in order to capture incoming sensor data with a clock phase synchronised to the phase of the sensor die clock. As the sensor dies output their data with half the sensor die clock frequency, the processing chain clock frequency is half of the one from the sensor die clock. With the typical operating frequency of the latter, the processing chain is clocked with 100 MHz being identical to the system clock frequency. However, this clock domain was separated from the system clock domain, as the clocking of the sensor dies and thus the processing chain in the Stack FPGAs can be altered with respect to frequency and phase. This was for instance applied for the PET-related RF interference reduction studies presented in chapters 5 and 6.

Encoding/Decoding of refCLK and synchronisation signals

The distribution of the refCLK and synchronisation signals between the CSU and the SDMs via a single optical line for each of them is done by encoding the synchronisation pulses with the clock signal. In the CSU, the combination of these signal types was implemented in a simple way. Whenever a synchronisation pulse is transmitted, the clock signal that uses a duty cycle of 50% per clock signal period is muted (gated) for exactly one clock cycle. On the SDM side, the SPU FPGA receives this combined signal, extracts the synchronisation pulse and restores the muted clock signal. The pulse extraction is performed using combinatorial logic to detect the missing clock cycle and, when detected, to generate a

synchronisation pulse. To restore the missing reference clock cycle, the combined signal is fed into a cascade of two clock-synthesis circuits being PLLs. These are configured to forward the clock signal and remove jitter on the input signal. A reference clock signal of 100 MHz allows configuration of the two cascaded PLLs to run their internal oscillator at their highest frequency of 1 GHz. This offers the best stability of the oscillating circuits with regard to an input clock signal with high jitter or even a missing clock cycle. As the jitter was too high when using only one PLL, a second one was added to form a cascade, yielding a continuous and jitter-free reference clock signal to be used by the DPC sensors and the SPU- and Stack-FPGA designs.

Stack FPGA design

Figure 3.11 represents a block diagram of the Stack FPGA design depicting the ctrl/status-data-related data flow and units. 21 modules can be addressed by the control PC via ctrl/status data transmission. 17 modules may send ctrl/status payload data in the downstream direction. The ctrl/status-related part of the PDPC subsystem is represented as a single module embedded into the HyperDAC FPGA design, as in- and out-coming PDPC ctrl/status data is handled by a protocol-wrapper and serialiser/deserialiser unit.
In fig. 3.12, the block diagram related to the PET data path is depicted. Incoming DPC sensor data is acquired by routing it to the PDPC processing chain through a unit capable of generating synthetic (dummy) sensor data. This dummy data generator (DDG) is part of the PDPC subsystem. An activation leads to the DDG being the data source to the processing chain instead of the data input path of the real sensors. The DDG can generates multiples of DPC sensor messages per time frame for all sensors of a sensor tile. Therefore, the stepping of the generator is in amounts of 16 DPC sensor messages per time frame. The stepping range covers 1 up to 63 data messages per sensor and time frame, leading to a maximum data message amount of 1008 per time frame. Furthermore, the DDG outputs a framing message per sensor die and time frame.

SPU FPGA design

The ctrl/status data path flow of the implemented SPU FPGA design is shown in fig. 3.13. The data path is distributed over the GbitE-, the system-, and

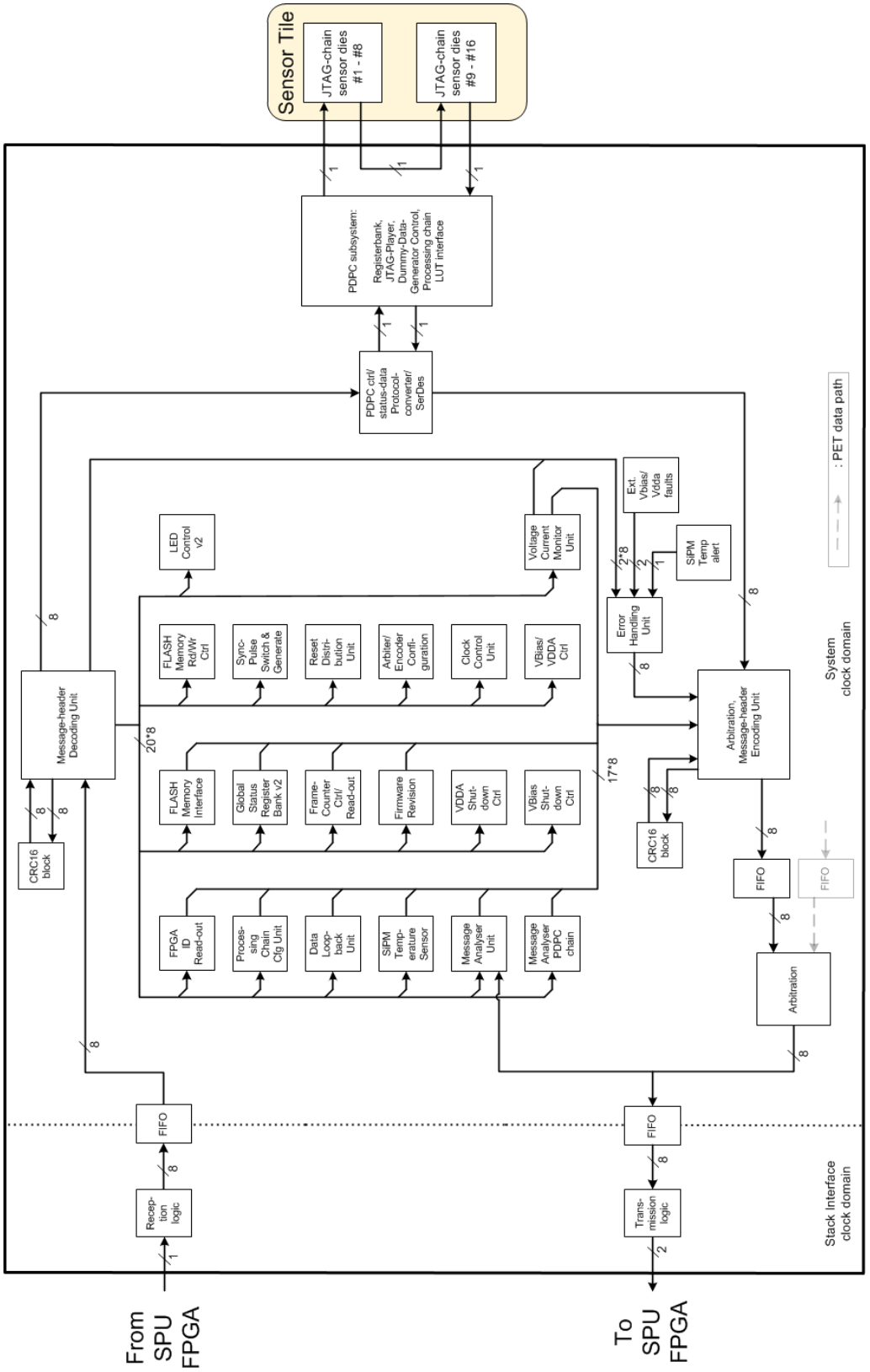


Figure 3.11: Control/status-related data path overview of the Stack FPGA design.

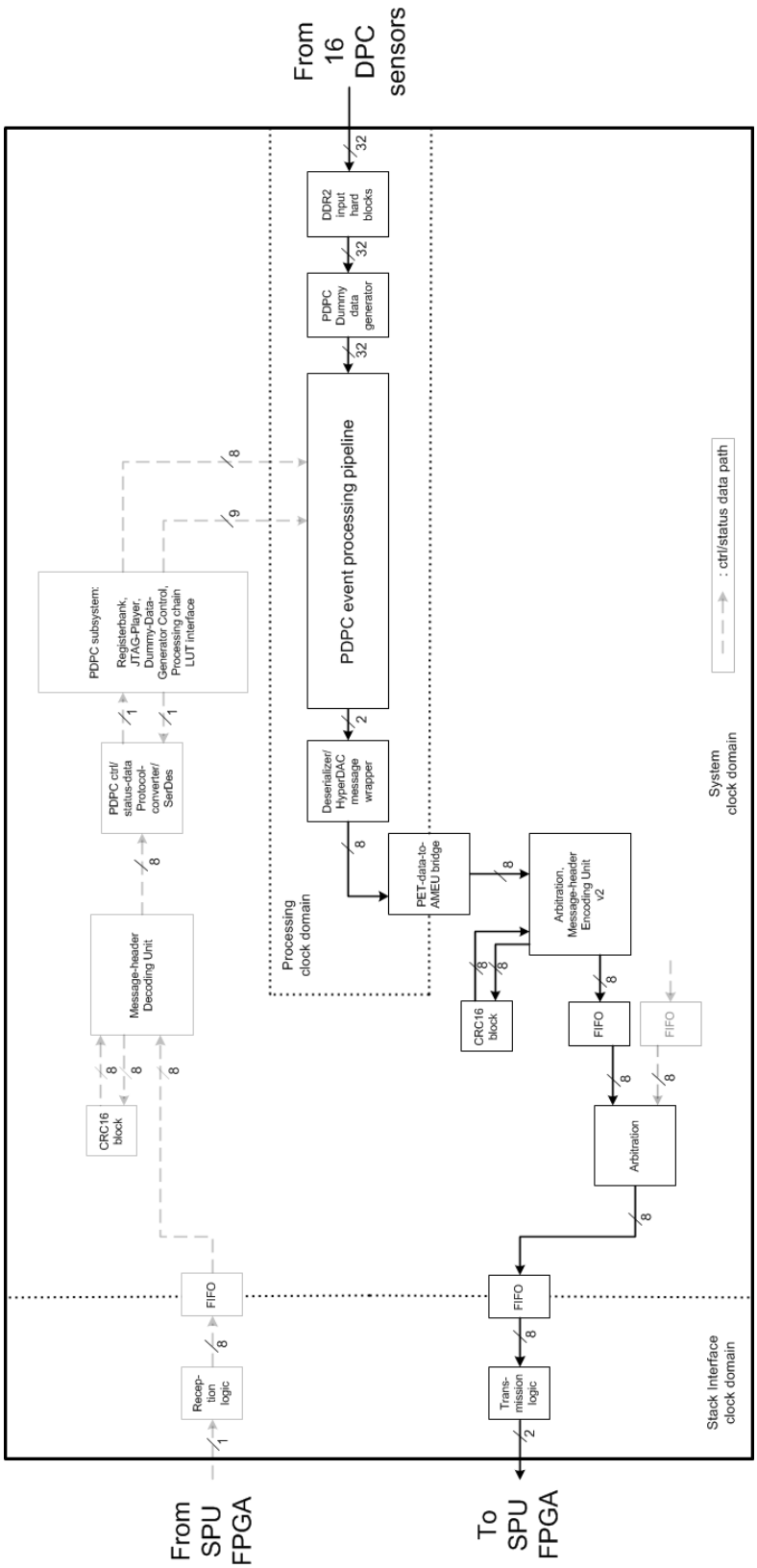


Figure 3.12: PET data path overview of the Stack FPGA design.

the stack-interface-clock domains. There are 23 different modules that can receive ctrl/status data from the upstream direction. Ctrl/status messages with destination to the stack FPGAs are forwarded by the message decoder via the data communication interface. 17 SPU-FPGA-internal modules and the error handling unit may send data in downstream direction. Analogously to the message decoders and encoders, the splitters verify the message header integrity of all messages originating from the stack FPGAs and only forward them into the ctrl/status or PET data paths upon successful verification.
The communication interface between the SPU- and Stack-FPGAs does not include congestion control mechanisms yet, meaning that in each direction, the receiver side has to make sure that incoming data can be stored. When input FIFOs cannot store a complete message any more, the message coming in via the communication interface needs to be discarded, which is an additional task done by the message type splitters in case of the downstream direction. As the bandwidth of the data path in the system clock domain is limited to 800 Mbit/s, the downstream data paths between the message-encoder-and-arbitration unit and the GbitE interface represent the bottlenecks of the acquisition platform implementation (see fig. 3.14). Thus, when the average data rate provided by all stacks is in the range between 800 and 1200 MBit/s, message congestion occurs in the FIFOs of the ctrl/status and PET data paths between the second-stage-arbiter and the data type splitters, depending on the data message type load (ratio of ctrl/status to PET data throughput). Data messages are then discarded by the data type splitters upon sustained bandwidth exceeding the data paths shared by message of same type (paths between the two arbiter stages) or/and the shared ctrl/status/PET data path between the second-stage-arbiter and the Gbit Ethernet interface.
As visualised in fig. 3.14, the PET data path of the SPU FPGA design so far only has bypass channels implemented in order to forward incoming PET data messages. However, mechanisms are implemented in the message type splitters which allow forwarding of PET payload data to future data processing chains or forwarding PET data messages via the bypass channels to be selected, or both.

CSU and RTU FPGA designs

The FPGA design of the Central Synchronisation Unit with respect to the ctrl/

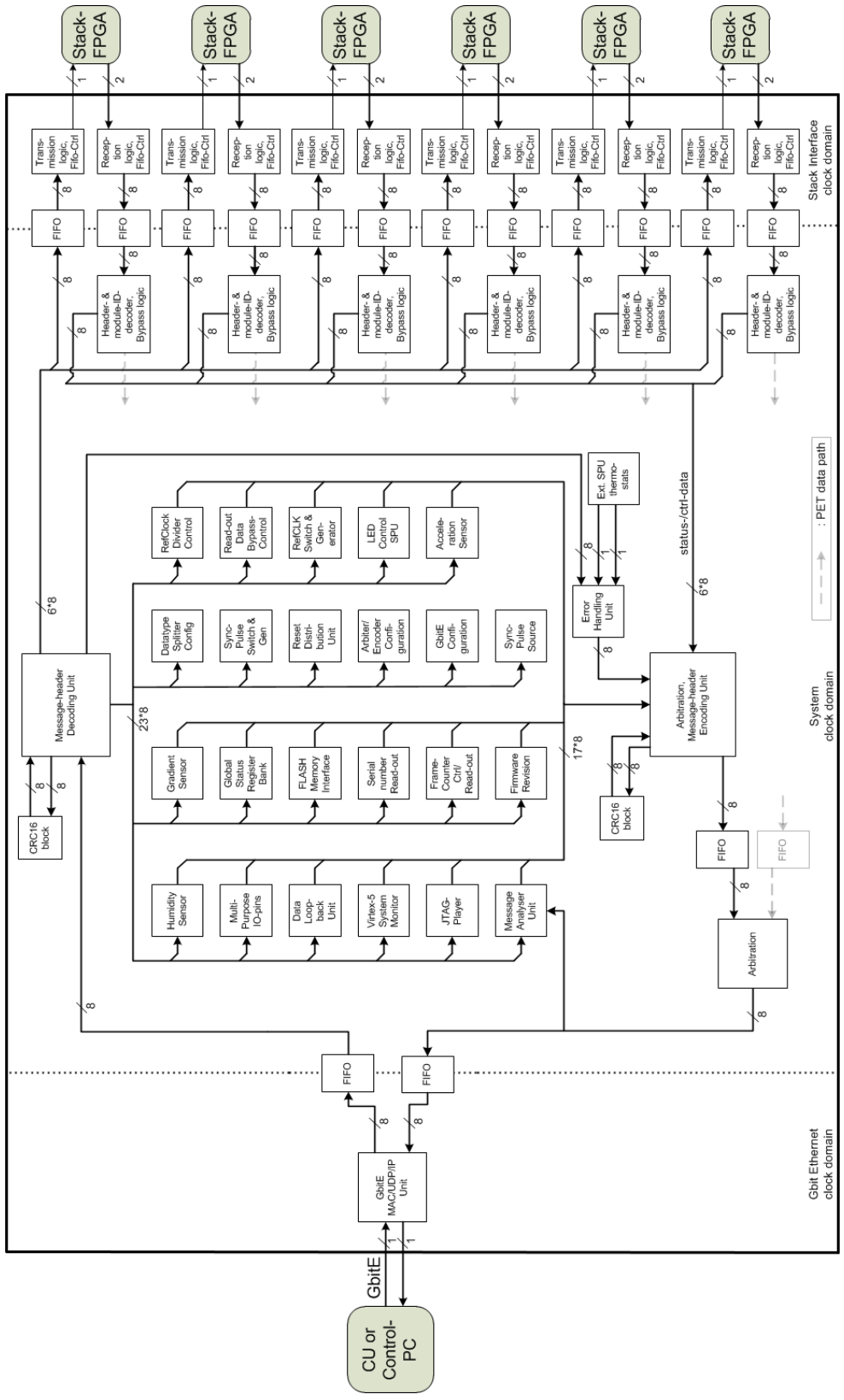


Figure 3.13: Control/status-related data path overview of the SPU FPGA design.

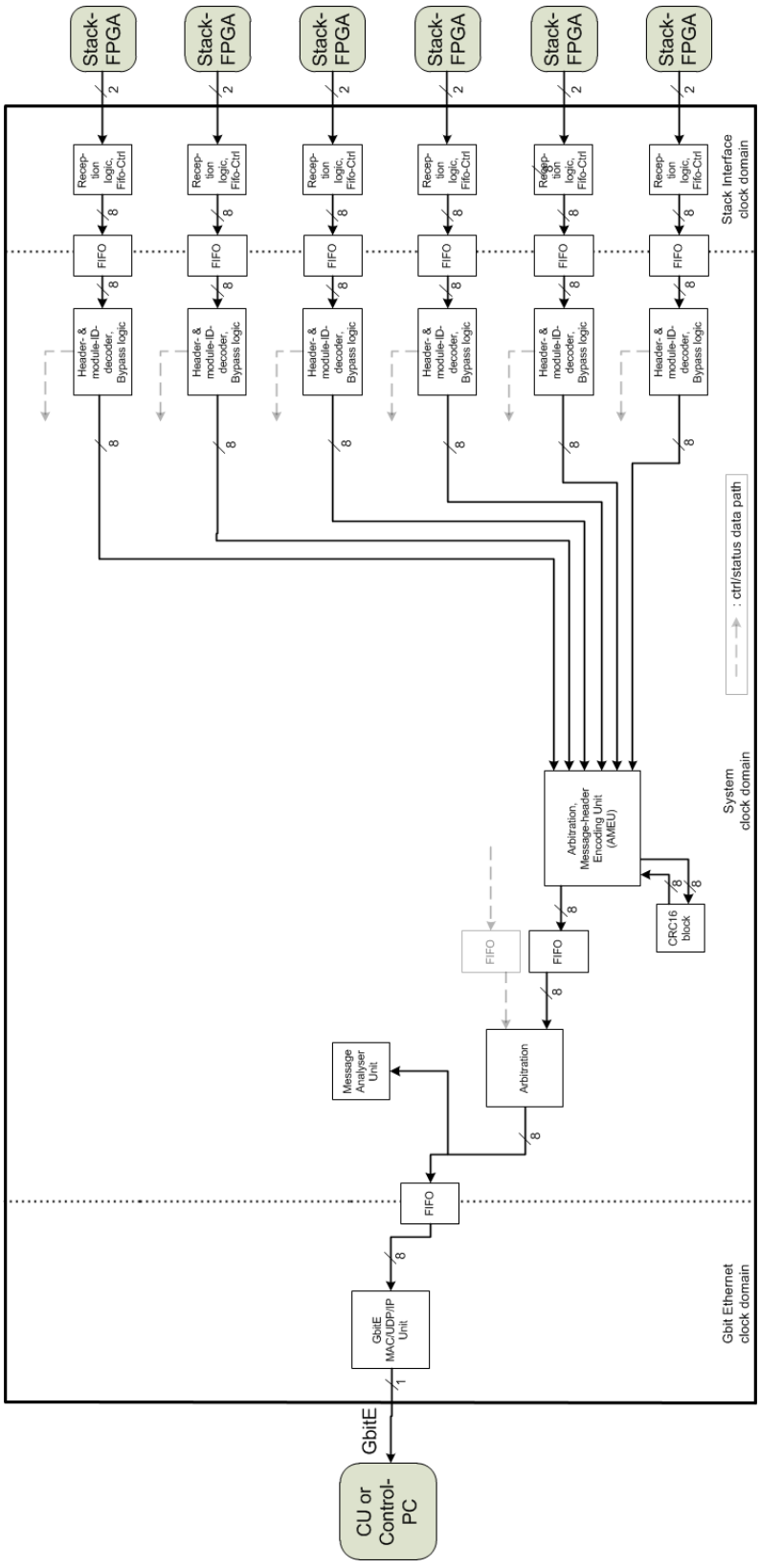


Figure 3.14: PET data path overview of the SPU FPGA design.

status data path is shown in fig. 3.13. 32 internal modules are able to receive ctrl/status data from the upstream data path and 22 internal modules plus the error handler can transmit ctrl/status data in the downstream direction. The modules located within the data path design are mostly those of the SPU FPGA as depicted in fig. 3.13 with some additional modules to offer CSU-specific functionality. These cover amongst others generation of the combined refCLK/synchronisation signaling and the transmission and reception of external electrical or optical trigger signals. A trigger signalling reception fulfilling a configurable trigger condition results in a ctrl/status message generation with time stamp information or can be used to generate and forward a new trigger to the CSU trigger outputs or to generate synchronisation pulses, if wished. This function is the main purpose of the remote trigger unit (RTU) that is located in the MRI control room where MRI trigger signals are forwarded optically to the CSU and the SDMs in the MRI examination room for synchronisation purposes. Examples for this application are introduced in more detail in chapter 4. The RTU is, similar to the CSU, based on a SPU board using dedicated daughter boards that are connected at the stack connectors. The RTU FGPA design is thus like the CSU FPGA design mapped on the Virtex-5 FPGA of the SPU board. A diagram of the RTU FPGA ctrl/status data path flow was omitted as it is similar to the one of the CSU FPGA design.

Control PC software "Hyperion"

The control PC software implements the modular and scalable approaches of the HyperDAC architecture by mirroring the "'Hyperion II^D topology with its nodes and node-internal modules of the DAPS software and the FPGA designs. Message header generation, processing and forwarding follow the same principles as described in section 3.2.1.2 and nodes, modules and their functions can be added/removed/modified analogously to implementation changes in the DAPS software and FPGA designs.

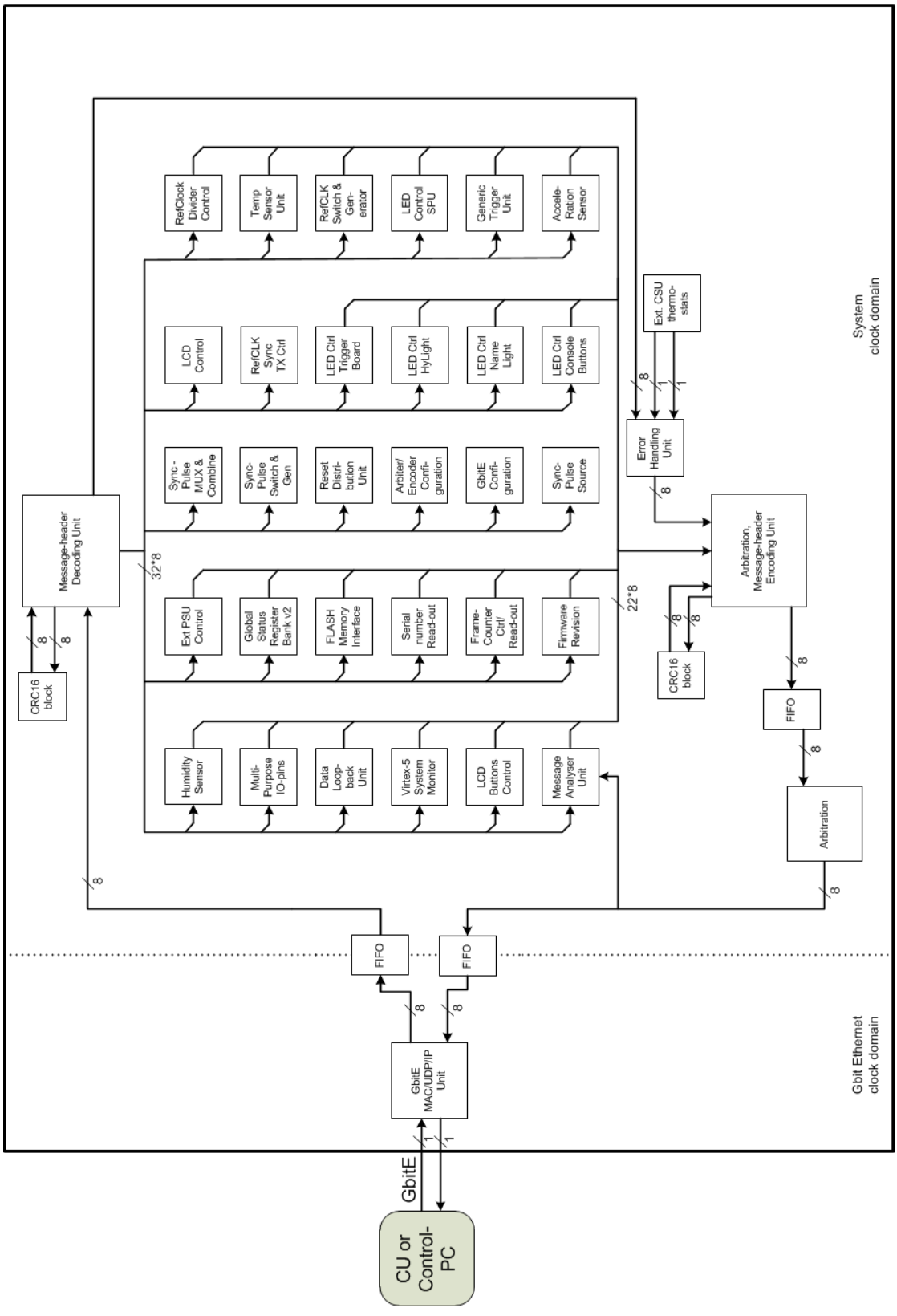


Figure 3.15: CSU-FPGA-internal communication infrastructure of the Central Synchronisation Unit

Design development environment and tools

VHDL was used as the hardware description language to implement the FPGA design. The design was developed using *HDL Designer* 2009, 2010.3 and 2013.1b (Mentor Graphics Corp, Wilsonville, Oregon, USA) as a design environment which offers graphical structural and behavioural design entry in addition to text-based programming. Graphical design entries result in VHDL code generated by HDL Designer. All FPGA designs were simulated with *ModelSim PE* 6.4 and 10.3b (Mentor Graphics). The designs were synthesised, placed and routed with *Integrated Software Environment* (ISE) 10.3, 11.5 and 13.1. (Xilinx Inc, San Jose, California, USA). To improve timing results, timing analysis and manual placement optimisations after the automated design placement and routing process were performed with *PlanAhead* 13.1 (Xilinx).

3.2.4 Measurements

In order to study the data acquisition of the FPGA-based platform with regard to its data message transmission behaviour, different measurement series covering a range of conditions were defined and performed. The measurements aim to provide an analysis of the data message transmission quality within the designed throughput range as well as beyond it. Within the platform's bandwidth range, no message loss or corruption is expected. If the stack provide data at rates lying beyond the bandwidth limitation of the SPU FPGA design, data messages are expected to be discarded.

To monitor the data transmission behaviour with respect to missing or corrupted data, a message analyser was implemented for the SPU FPGA design. The analyser tracks the data traffic in the downstream direction between the output of the second arbiter stage and the input of the GBit Ethernet unit (see fig. 3.13). Different fault types are detectable by the analyser and a careful design simulation of the analyser was performed to ensure that the detection operates properly for different kinds of inconsistencies. The latter are summarised in table 3.2. All faults except P and Q originate from messages directly read by the analyser. The faults P and Q are provided to the analyser by the data

type splitters. The splitters' CRC analysis of the header and the payload help to determine, if data corruption has occured along the message transmission path between the stack- and the SPU-FPGAs during MRI operation. For all measurements, the message payload-CRC generation in the Stack FPGAs was activated and the payload-CRC checksum was verified by the data type splitters and reported to the message analysers. Furthermore, the analyser counts all ctrl/status and PET data messages over time with two separate counters for each message type and outputs the number of messages autonomously at programmable intervals between 0.3 s and 10.7 s. A detected fault is stored in FPGA-internal memory as a 72bit-wide entry with information about the detection time, stack and module IDs, and the sequence number. The memory has space for 2048 entries and the storage of detected faults is stopped when the memory is full. However, the analyser can be configured to automatically transmit the memory content upon a threshold exceedance. This allows to continuously write newly detected faults into memory after former memory entries have been transmitted to the control-PC. For measurements done in the region of the bandwidth limitation, the missing sequence number fault detection was deactivated in order to avoid permanent memory read-out due to message rejection, as the transmission of the stored analyser data of over 18 kbytes requires bandwidth along the shared downstream data path which distorts the actual measurements. However, every other fault type was tracked by the analyser measurements beyond the saturation of the SPU FPGA data path.

For the measurements, PET data was generated with either the dummy data generators (DDG) located in each Stack FPGA design and or by using ^{18}F to generate real PET data with the DPC sensors. The DDGs were used to perform measurements with predictive, synthetically generated PET data. The amount of data to be generated is software-controllable and the throughput range covers the complete bandwidth of the FPGA-based acquisition platform. The amount of messages to be generated per time frame by a DDG for each of the 16 input channels of the PDPC processing chain can be set between 1 and 63. The messages are sent in a regular (non-random) time interval within each time frame. A DDG-generated message has the same structure as the one from a DPC sensor message, but the DDG-message-internal data does not contain meaningful en-

Table 3.2: Overview of the fault types detectable by the HyperDAC message analyser

Fault type	Fault code	Fault description
Invalid preamble	E	Unexpected preamble sequence detection
Unexpected sequence number	M	Consecutive messages of same source not having consecutive header sequence numbers
Invalid header-CRC	T	Calculated checksum does not match the detected one
Invalid trailer	A	Unexpected trailer sequence detection
Invalid header-CRC (DTS)	Q	Calculated checksum does not match the detected one
Invalid payload-CRC (DTS)	P	Calculated checksum does not match the detected one

ergy or time-stamp values, as these are not evaluated for the data transmission tests. The resulting range of messages sent to the processing chain is between 16 and 1008 messages per time frame. The pipeline saturates at a number of 32 messages for each of the 16 input channels which corresponds the maximum of 512 processable sensor die messages per time frame.

Although the measurements could be done with a single SDM to study the behaviour of the FPGA-based platform, all measurements are performed using all SDMs of the PET insert. This increases the statistical accuracy of results obtained per measurement. With the modules operating synchronously, singles and coincidences-rates can be determined in addition to data transfer rates for the measurements series done with radioactivity. Ctrl/status data flow in the downstream direction is generated by requesting environmental information which we usually request during PET and PET/MR measurements. The information type, firmware module location and message length in the downstream direction at the input of the SPU encoders are summarised in table 3.3. These sensors are usually read out at a rate of 1 s which is sufficient to monitor the operating environment of the PET insert.

For the measurements with radioactivity, the system configuration parameter set was set to one typically used for PET and PET/MR measurements with the insert when acquiring images at high count rates. This serves comparison pur-

Table 3.3: Overview of the status information read for different environmental sensors of the PET insert. The message lengths refer to messages at the SPU message encoder inputs

Module name	Information	FPGA	downstream message length, #messages
Virtex-5 System monitor	FPGA core voltages and temperature	SPU	66 bytes, 1
Humidity sensor	Humidity, temperature and dewpoint	SPU	15 bytes, 2
Stack & LDO temperature sensors	Temperature below the interface boards and the SPU LDO	SPU	6 bytes, 7
Sensor tile temperature sensor	Temperature on backside of sensor tile	Stack	11 bytes, 1
DPC sensor voltages & currents	Vbias, Ibias, VDDA, IDDA of DPC sensors	Stack	21 bytes, 1

poses with results reported in [158, 159]. Regarding the DPC sensor over-voltage setting, inhibit memory configuration and general configuration parameter set, 20% of the SPADs with the highest dark count rates were disabled and the over-voltage was set to 2.5 V. The sensor die validation time was set to 4 clock cycle times (t_{CK}) (1 $t_{CK} \widehat{=} 5$ ns) and the DPC sensor integration time was set to 17 t_{CK}. The validation threshold was set to 37.1 ± 12.8 photons (setting 0x50). The acquired PET raw data was processed on-line using the Centre-of-Gravity with Adaptive Corner Extrapolation (CoG-ACE) positioning algorithm to perform PET singles clustering by the data acquisition and processing server as described in [158]. The processing software calculates singles and coincidences rates during the measurements which is used to correlate them with the message and raw data rates.

HyperDAC PET data messages are considerably larger than the ctrl/status messages listed in table 3.3. When leaving the Stack FPGAs, they have a minimum size of 249 bytes containing 16 framing messages that are always generated during raw-mode operation of the PDPC processing chain. 25 bytes are used by HyperDAC and PDPC header information plus payload-CRC. For each DPC message content, 14 bytes are used. Consequently, the maximum message size with 512 DPC sensor data messages and 16 framing messages equals 7417 bytes.

For all measurements, the amount of analysed messages were autonomously transmitted to the control PC at constant rates by the SPU message analysers and faults detected during DDG- and radioactivity-based PET measurements were plotted for each PET measurement. This made it possible to analyse the data transmission behaviour against the SDM data rates (and coincidence and singles rates for scans with ^{18}F) obtained by the acquisition server.
With the data generators, the bandwidth limitation in the SPU FPGA design is reached when setting the data generators to output 23 DPC sensor messages per time frame. The resulting message size at the output of the SPU arbiter/encoder block per PET data message is $23 * 224\,\text{bytes} + 251\,\text{bytes}$ for framing-message/header/trailer information $= 5403\,\text{bytes}$. With six PET data messages transmitted per time frame, the data rate equals 98.93 Mbytes/s. With the aforementioned data processing and DPC sensor settings including a validation threshold setting of $0x50h$, this DDG setting applied to all SDMs of the PET insert corresponds to a coincidence rate of approx. 300 kcps at an activity of 55 MBq in a mouse-sized hot-rod phantom as determined in [158]. Beyond this activity, PET data messages with resulting average sizes larger than 5403bytes are discarded at an increasing rate with increasing radio-activity. At a data generator setting of 16 times 32 DPC sensor messages per time frame and a maximum throughput of 100 MB/s in the SPU FPGA, the PET data message rate per time frame decreases from 6 to

$$\frac{x \times 7418\,B}{327.68\,\mu s} = 100\,MB/s \iff \frac{100\,MB/s \times 327.68\,\mu s}{7418\,B} = 4.17 \tag{3.5}$$

This is the lowest PET data message rate per time frame of $327.68\,\mu$s reachable by a PET module when all PDPC processing chain input channels of all stacks are saturated.

DDG-driven data transmission measurements

Measurements with the DDGs are performed in order to study the transmission behaviour under different ratios of ctrl/status and PET data messages in the downstream direction. Each measurement began with the DDG setting of 32 messages per sensor and time frame and was decremented down to one every four

seconds which yielded approx. 12207 time frames of PET data with a same DDG setting. Two different ratios of PET and ctrl/status messages transmitted in the downstream direction were generated by setting the environmental read-out rate to 1 *s* and to 0.1 s. PET data message rejections in the SPU FPGA were tracked by the message analyser to determine the message rate at which the rejection begins. The tracking of missing PET data messages was deactivated for measurements up to the PDPC chains' bandwidth saturation to be able to store any other error type recognisable by the analyser. The analyser's memory content is read out after the end of each measurement to avoid any distortion of the measurement conditions due to high message rates due to potentially filled memories. The sum of analysed healthy PET and ctrl/status data messages,however, is provided every 0.67 s during the measurement.

PET measurements with ^{18}F

As a next step, the data transmission was studied under realistic PET measurement conditions. To obtain complementary results under measurement conditions used for PET system performance studies [159] and software-based PET data processing throughput studies [158], an ^{18}F activity of 85 MBq located in a vial was used as a starting point. No particular phantom type was required as the activity was solely used to trigger PET data. The data transmission behaviour was tracked until the activity decayed down to 2.4 MBq. The missing-sequence-number-tracking was deactivated to allow detectability of other faults while not distorting the PET measurement conditions due to repetitive message analyser memory data transmission in combination with activated autonomous memory readout. Analogous to measurements done in [159, 158, 125], the environmental sensor read-out was done once per second.

Data transmission under simultaneous PET/MR imaging conditions

To study MRI-related interferences on the data transmission of the FPGA-based platform with regard to data loss or corruption, PET measurements were performed while the 3-T MRI executed sequences to yield repetitive switching gradient fields and RF excitation. Particularly the PET message header- and payload-CRC checking performed after message transmission from the Stacks to the SPU FPGA is of interest, as the messages are transmitted over LVDS lines and stack

connectors. Possible MRI-related disturbances of the PET data transmission are studied separately for MR gradient field switching in X, Y and Z-directions and RF field excitation. The MR sequence presented in [160] was used to generate gradient field switching for three different field strengths of 10, 20 and $30\,\mathrm{mT\,m^{-1}}$ with varying switching duty cycles and slew rate (SR) variations up to $200\,mT\,\mathrm{m^{-1}\,s^{-1}}$. The latter represents the maximum SR achievable in high SR mode with the dual-gradient-amplifier installation of the 3-T MRI.
A T_2-weighted Turbo-Spin-Echo (TSE) sequence applying extensive RF excitation (T_R/T_E: 1500/60 ms, TSE factor: 44, acq. matrix: 100×80) was applied using the gamma-transparent mouse RF coil of the PET insert in order to study the PET data transmission with regard to possible RF-related interferences. Two measurement sets were performed: For the first one, real PET data was generated with ^{18}F. On-line singles and coincidence processing using the DAPS SCP software (Singles Clustering scheme: Center-of-Gravity, central Hit using all direct neighbour SiPM pixels [142, 158]) was performed to plot the Singles and Coincidences rates. For the second PET/MR measurement, PET dummy data generators were used to generate synthetic PET data at a defined data rate. The latter was used to yield a throughput close to saturation to increase the likelihood of faults and their detection. At the end of each measurement, The message analysers' internal memories in the SPU FPGAs were read out and their content, if any, checked for faults occurring during active MRI operation.

3.3 Results

3.3.1 Implementation

The VHDL description of the Stack-, SPU-, and CSU-FPGA designs result in more than 363300 lines of code (exlcuding the RTU FPGA design which is similar to the CSU FPGA design). Table 3.4 gives an overview of the FPGA resources needed to implement the different designs.

Table 3.4: FPGA resources used by the different FPGA designs. The resources offered by the FPGA models were added for comparison purposes.

	V5 FX70T	SPU	CSU	RTU	S6 LX45	Stack
#Slice registers	44800	20787	19357	15556	54576	14971
#Slice LUTs	44800	23208	27328	21742	27288	17336
Used as logic	44800	21810	26210	20665	27288	15423
Used as memory	13120	1224	1004	990	6408	946
# BlockRAM	148	101	39	36	116	81
BlockRAM Memory used [KB]	5328	3366	1242	1188	2088	1458

3.3.2 DDG-driven data transmission measurements

Figures 3.16 and 3.17 summarise the measurement results obtained for one SDM. The results for all other nine SDMs of the PET insert were very similar. The ctrl/status data rate measurement points vary for each SDM, as each ctrl/status message in the downstream direction is triggered by a readout of the Control PC with the latter not being timing-accurate. In fig. 3.16 (d), the PET data message rate per time frame is shown. It decreases by $\geq$23 times 16 DPC sensor messages per time frame and reaches an average of 4.415 PET data messages per time frame when the processing chains are saturated. For both measurements at different read-out rates, no faults were detected by the message analyser.
The ctrl/status data rate in fig. 3.17(c) reveals a larger variation between 0 and 5 s and between 90 and 100 s, whereas the PET data message rate remains constant over the entire time. This is likely to be a result of operating-system-related context switching resulting in delays and then grouping ctrl/status data messages together and sending them out at once instead of maintaining a delay of 100 ms between messages.
Figures 3.18 and 3.19 present the results for throughput measurements covering the SPU FPGA bandwidth and when saturation is entered. The latter is obtained with the generators sending 24*16 DPC sensor messages per stack and time frame to the PDPC processing chains. Only missing sequences numbers are tracked by the analyser at this point and were stored until its memory became full. No other faults and missing messages were detected throughout the entire measurement.

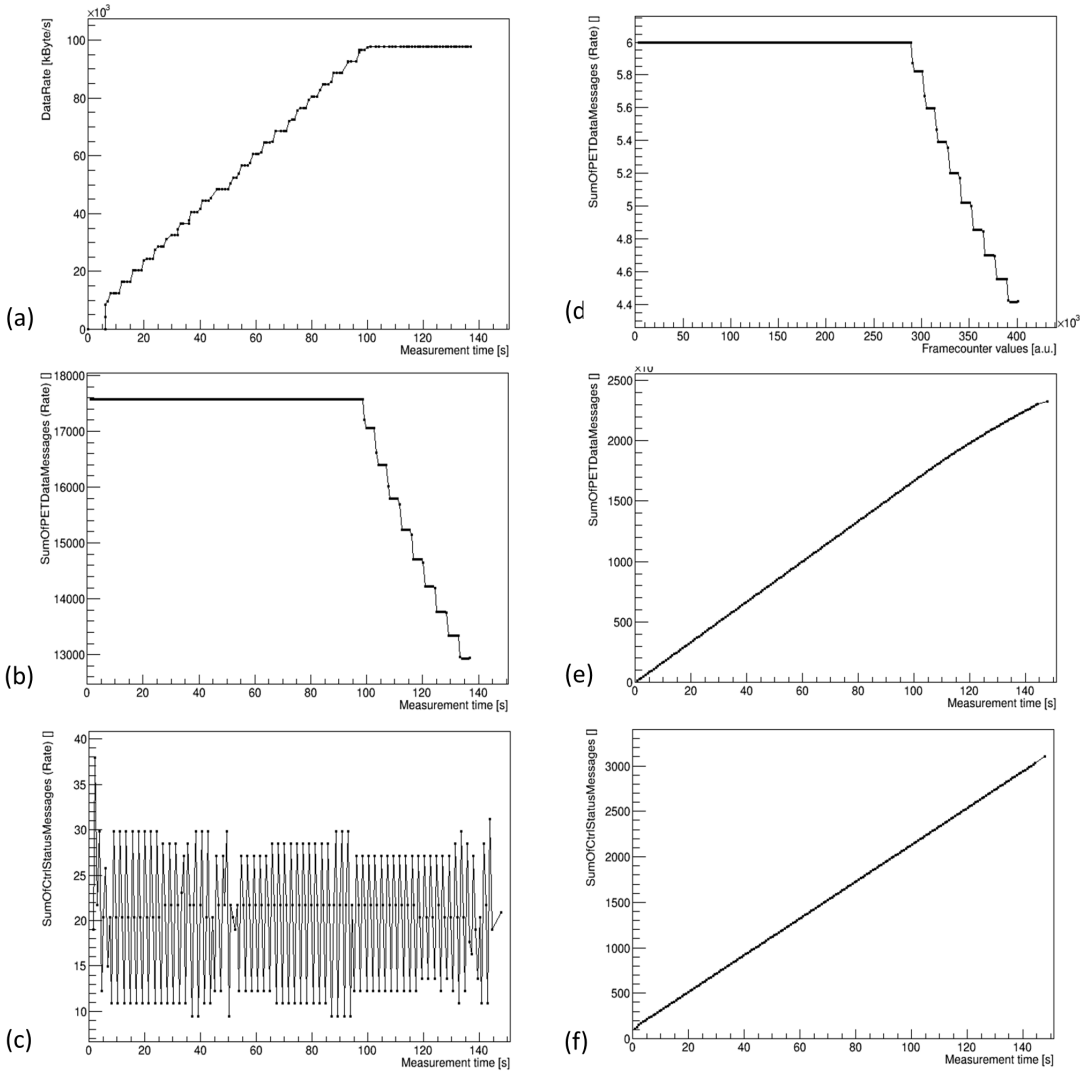


Figure 3.16: throughput easurement results of a single SDM covering the PDPC processing chain bandwidth and ctrl/status data read-out performed in 1 s intervals: (a) shows the data rate at the DAPS, (b) the PET data message rate, (e) the cumulative PET data message amount, (c) the ctrl/status data message rate, (f) the cumulative ctrl/status data message amount. (d) visualises the PET data message rate per 327.68 μs time frame

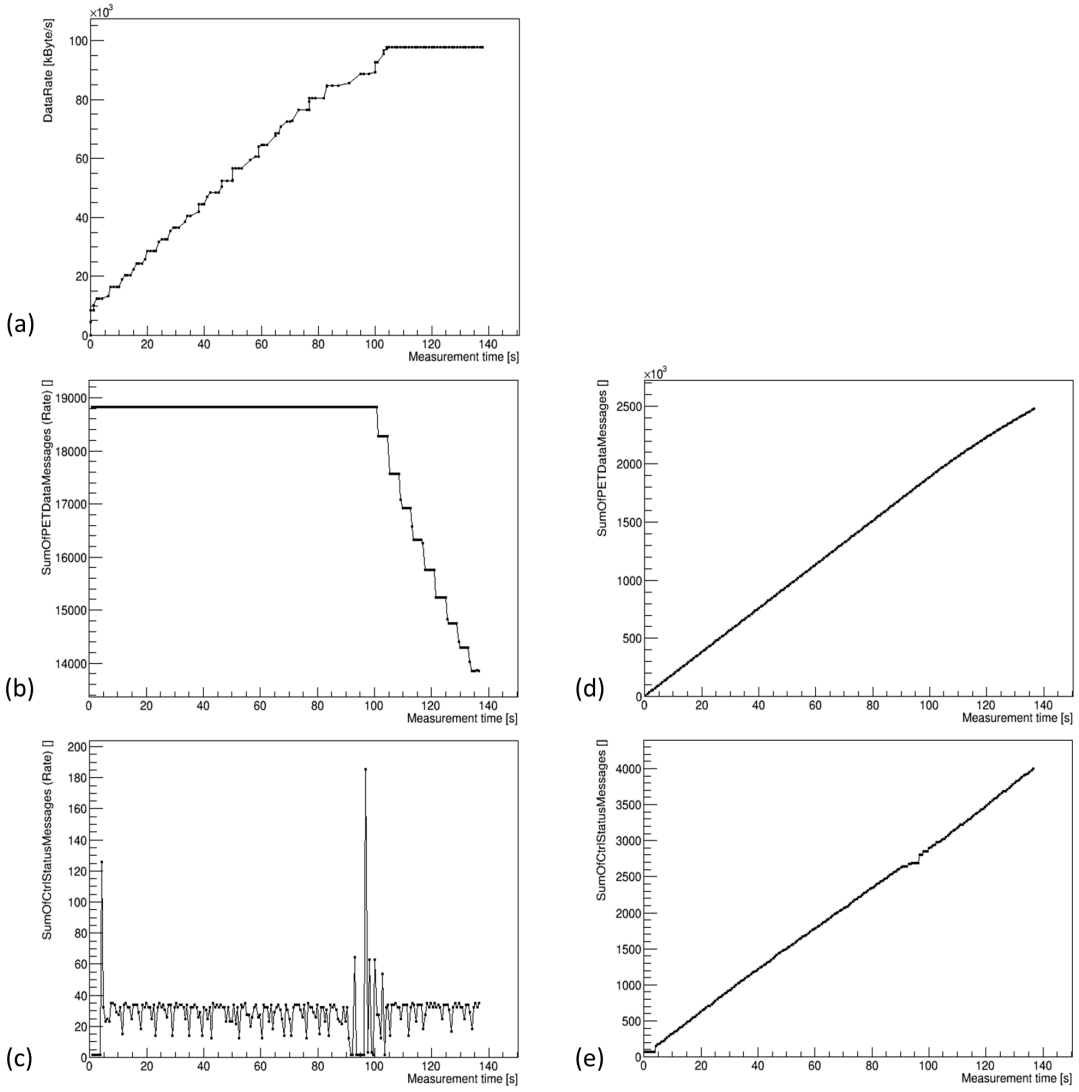


Figure 3.17: Throughput measurement results of a single SDM covering the PDPC processing chain bandwidth and ctrl/status data read-out performed in 100 ms intervals: (a) shows the data rate at the DAPS, (b) the PET data message rate, (e) the cumulative PET data message amount, (c) the ctrl/status data message rate, (f) the cumulative ctrl/status data message amount. (d) visualizes the PET data message rate per 327.68 μs time frame

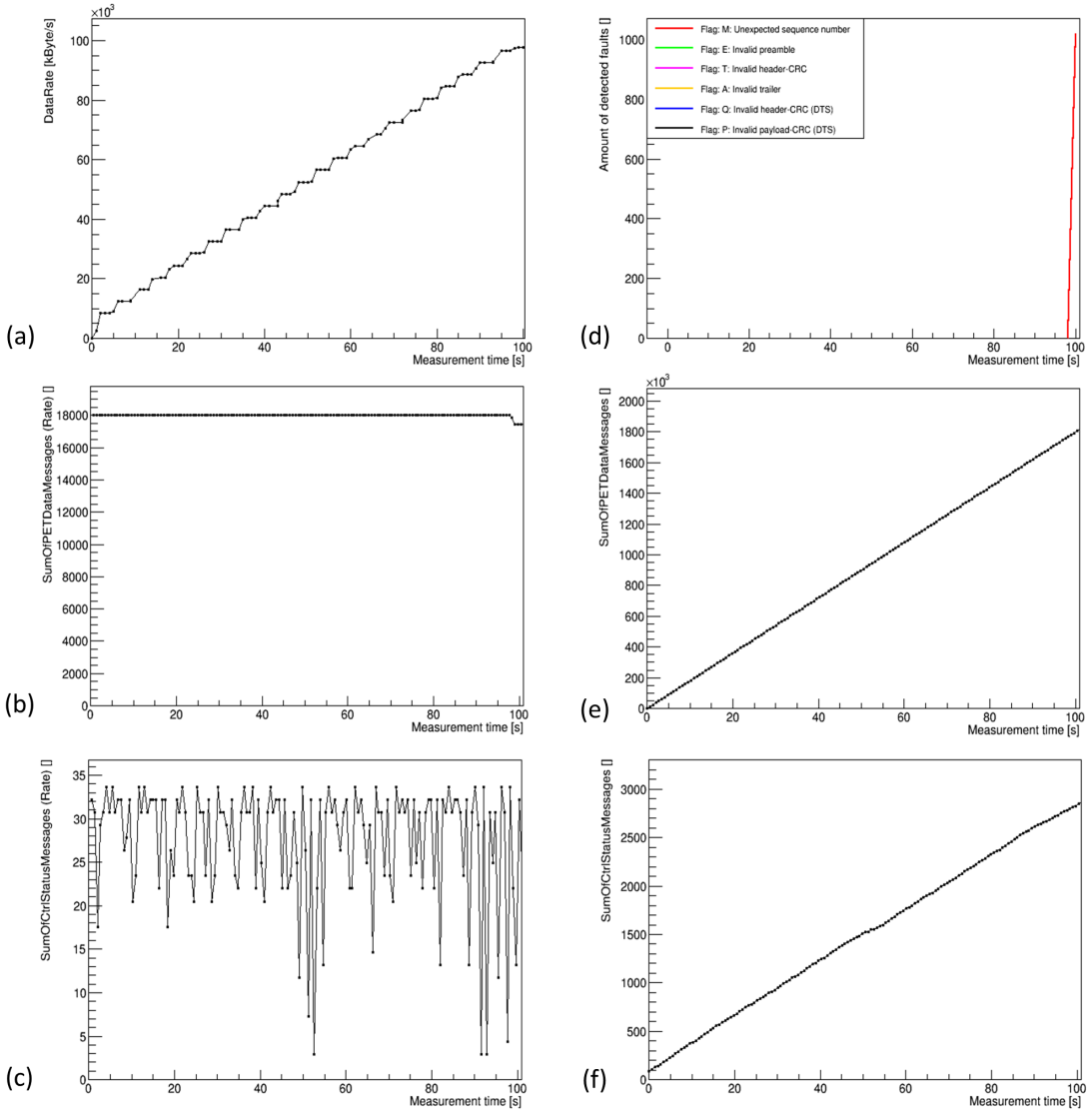


Figure 3.18: Throughput measurement results of a single SDM covering the SPU FPGA bandwidth and ctrl/status data read-out performed in 1 s intervals: (a) shows the data rate at the DAPS, (b) the PET data message rate, (e) the cumulative PET data message amount, (c) the ctrl/status data message rate, (f) the cumulative ctrl/status data message amount. (d) depicts the message analyser detected errors. No faults detected apart from the expected missing messages occurring beyond the bandwidth limitation.

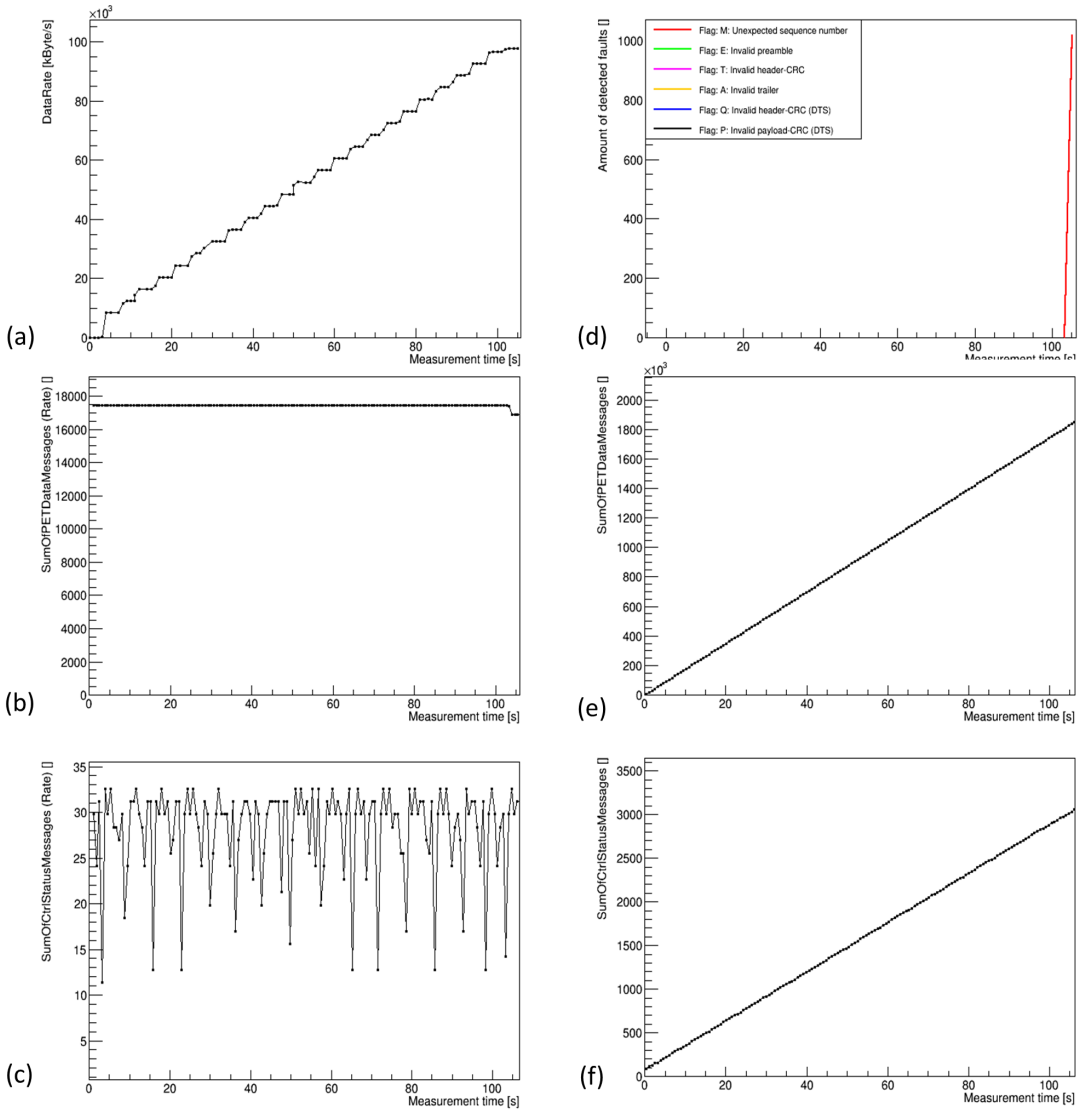


Figure 3.19: Throughput measurement results of a single SDM covering the SPU FPGA bandwidth and ctrl/status data read-out performed in 100 ms intervals: (a) shows the data rate at the DAPS, (b) the PET data message rate, (e) the cumulative PET data message amount, (c) the ctrl/status data message rate, (f) the cumulative ctrl/status data message amount. (d) depicts the faults detected by the message analyser. No faults detected apart from the expected missing messages occurring beyond the bandwidth limitation.

3.3.3 PET measurements with ^{18}F

Diagrams summarising the measurements obtained with SDM 3 as an example during the measurement with ^{18}F are shown in fig. 3.20 for an activity range between 85.1 MBq and 47.8 MBq (shown in fig. 3.20(a)). Down to an activity of 68 MBq, the SDM 3 operates in saturation at a data rate of approx. 97.6 MB/s and enters the bandwidth range of the SPU FPGA for lower activities as depicted in fig. 3.20(b). The data rate fluctuations provided by the acquisition server and Hyperion vary irregularly which is related to the high data load provided to the acquisition software. As shown in fig. 3.20(c), the PET data message rate increasing with decreasing activity until the SPU FPGA data path is not saturated any more. The ctrl/status data message rate remains constant throughout the shown measurement time. fig. 3.20 (e) and (f) depict faults detected by the message analyser. Between the measurement time range of 150 s and 1200 s, invalid header-CRC values were detected by the message data type splitters. The detection rate related to invalid header-CRCs decreases to a point where no more header-CRC faults are detected. Moreover, PET data messages with an invalid preamble were detected. The time frame where invalid message preambles were detected covers the range during which unexpected sequence numbers related to messages of the message analyser itself were detected (see fig. 3.20 (f)). After 1200 s of measurement time, no more faults other than expected missing PET data messages, whose detection was deactivated, where detected. To compare the PET data message rate during the ^{18}F measurement with the one of the measurement with the data generator (fig. 3.16(d)), the rate was additionally plotted for time frame periods as shown in fig. 3.21. The average message rate approaches six messages per time frame, indicating that the SDM is not operating in saturation any more.

The coincidence rate at 85.1 MBq was indicated by the the control PC software to be approx. 150 kcps, at 68 MBq (where SDM 3 leaves saturation) is was 170 kcps, and at 47.8 MBq it was 140 kHz. At the end of the measurement set (tracer activity of 47.8 MBq), the data acquisition software crashed and a further data set was acquired. The results for this measurement are visualised in fig. 3.22. Throughout this measurement period, no further errors including missing sequence numbers of PET data messages were detected by the message

analyser.

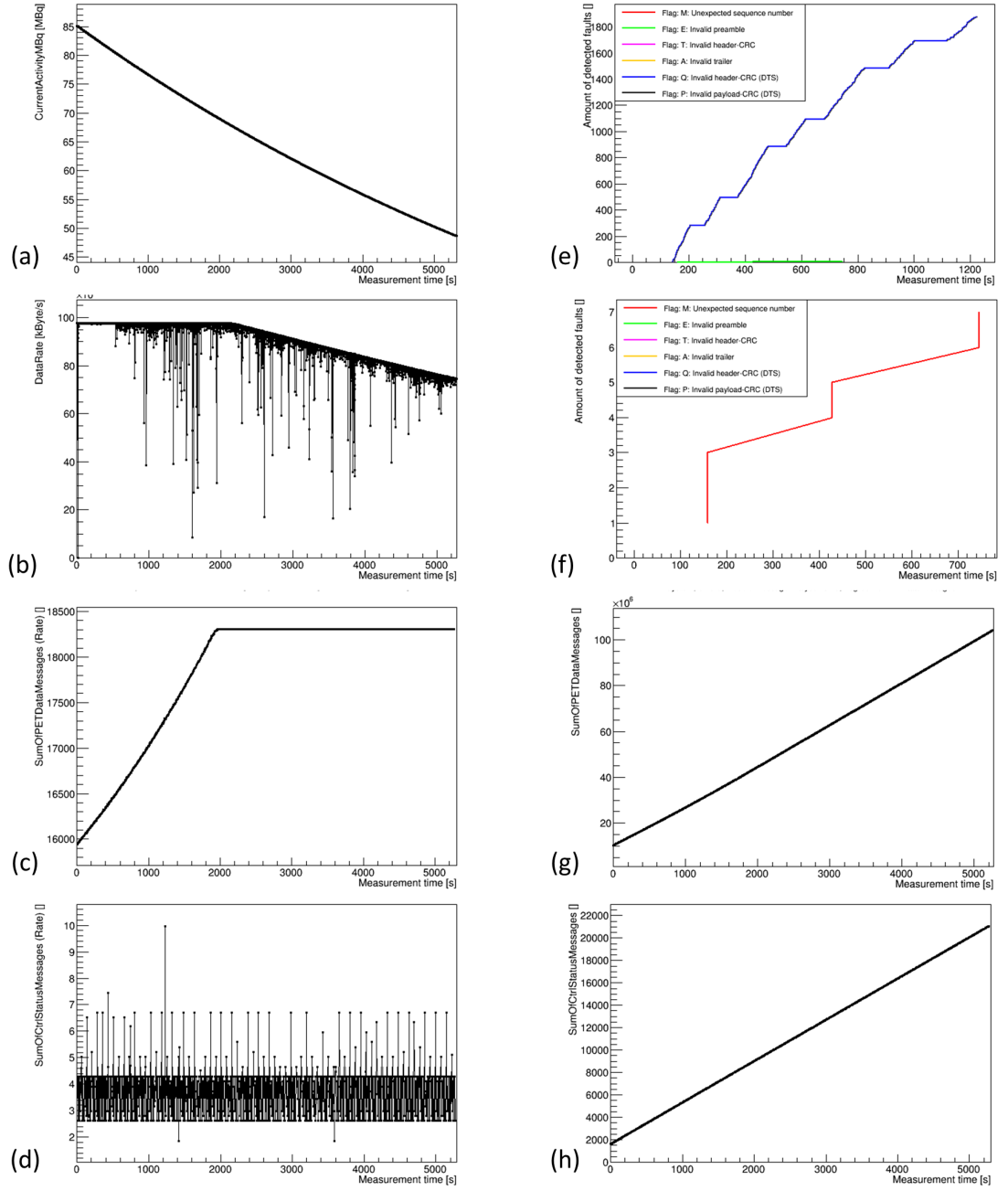


Figure 3.20: Measurement results of SDM 3 for the ^{18}F measurement (activity range: 85.1 MBq down to 47.8 MBq): (a) shows the isotope decay curve,(b) the total data rate of SDM 3,(c) the PET data message rate,(g) the cumulative PET data message amount,(d) the ctrl/status data message rate, (h) the cumulative ctrl/status data message amount.(e) depicts header-CRC faults detected by data type splitters (reported to the message analyser) and message preamble faults of PET data messages.(f) visualises missing messages from the message analyser itself.

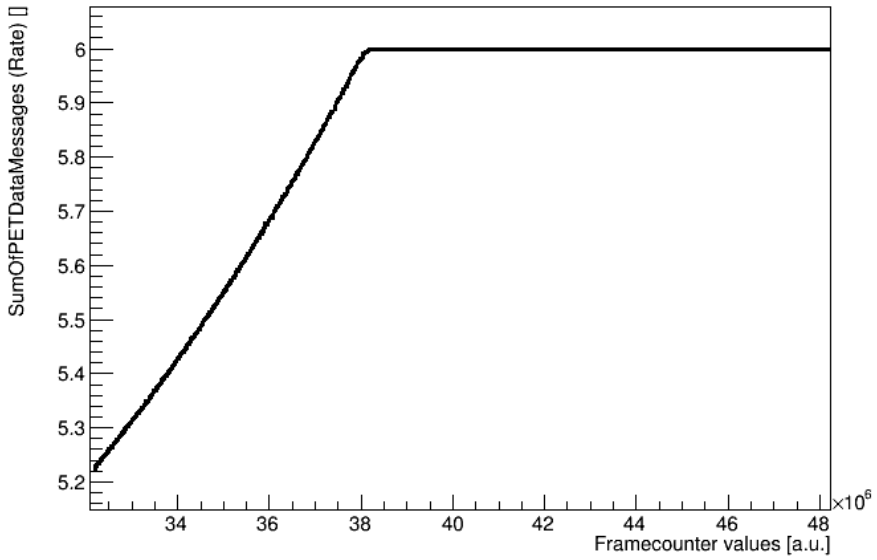


Figure 3.21: PET data message rate per time frame provided by SDM 3 during the ^{18}F measurement (activity range: 85.1 MBq to 47.8 MBq): A transmission of six messags per time frame indicates that the SDM does not operate in saturation anymore.

For the time period between 15800 and 17200 s (23.3 min), the DAPS did not acquire the SDM data. This behaviour holds for all other SDMs, too. While most of the measurement points are missing for this period, the sum of PET data and ctrl/status data messages provided by the analyser however demonstrates that data left the arbiter/encoder block in the SPU FPGA throughout this time without any detected faults.

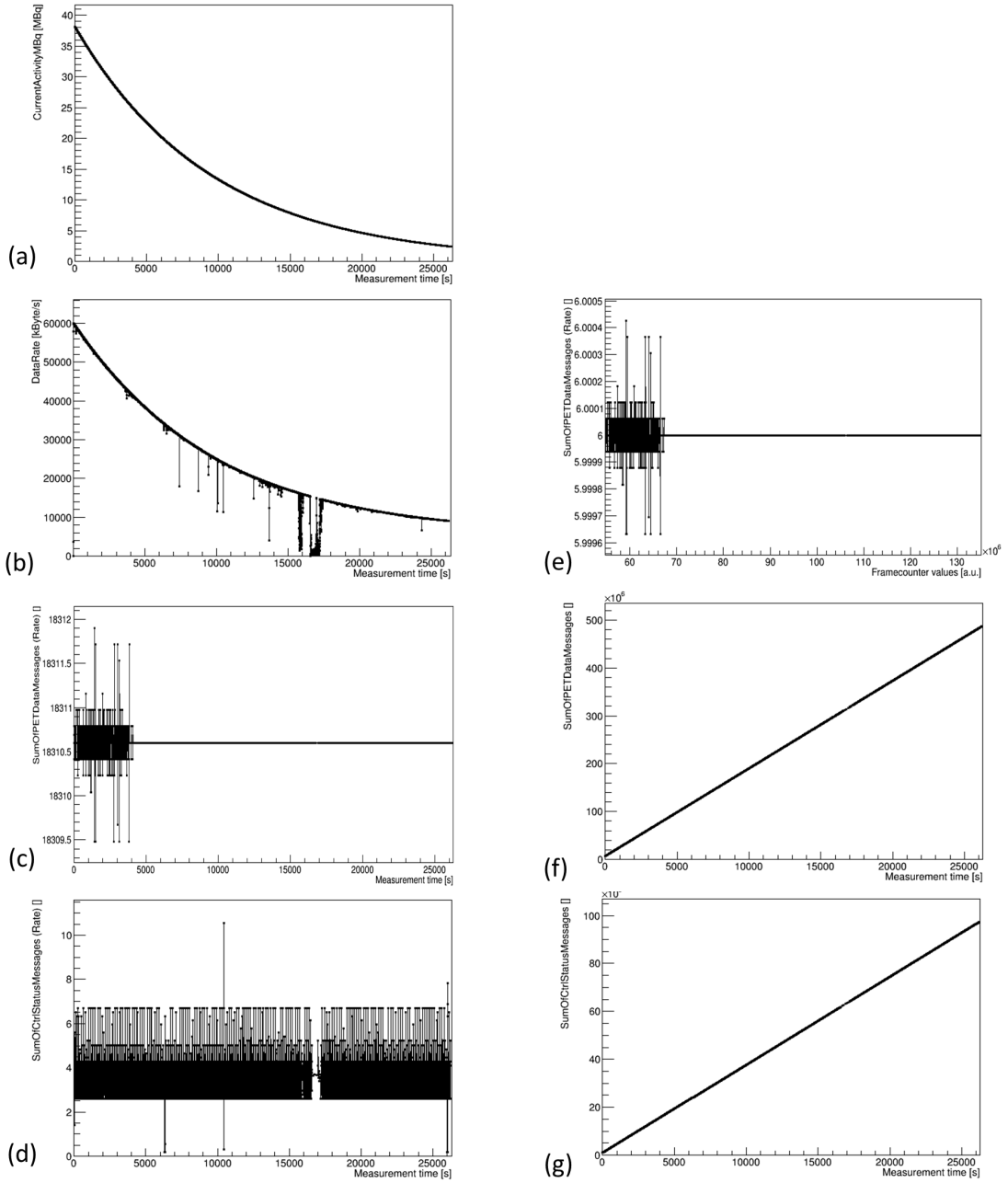


Figure 3.22: Measurement results of SDM 3 for the ^{18}F measurement (activity range: 38.1 MBq down to 2.4 MBq): (a) shows the isotope decay curve,(b) the total data rate of SDM 3,(c) the PET data message rate,(f) the cumulative PET data message amount,(d) the ctrl/status data message rate,(g) the cumulative ctrl/status data message amount. (e) shows the PET data message rate for units of time frames.

3.3.4 Data transmission under simultaneous PET/MR imaging conditions

The ^{18}F activity present in the iso-centre of the PET FOV was 26.5 MBq (distributed in 40 ml within a Falcon tube) at the beginning of the first PET/MR measurement. During the 12-minute-long PET measurement, Y, X, Z gradient switching and RF excitation were performed over time periods as depicted by the shaded areas in all the plots of fig. 3.23. Not a single fault was detected by the data message analysers of all SDMs during the PET/MR measurement. As a example, information of SDM 3 about data, message amount and message rates were visualised in fig. 3.23, whereas information about Singles and Coincidences applies to the complete PET insert.
For the second measurement, the dummy data generators were configured to generate 16x32 PET messages per time frame and stack, leading to a data rate in the range of 96 Mbytes/s as determined by the data acquisition server. Here, the SCP software was not used for Singles and Coincidences information, as the generated Hit data does not contain bit patterns leading to Singles and Coincidences. As for the ^{18}F driven measurement, no faults were detected by the message analysers during the entire 13.3-minutes-long PET measurement. Measurement information provided by SDM 3 are shown in fig. 3.24.

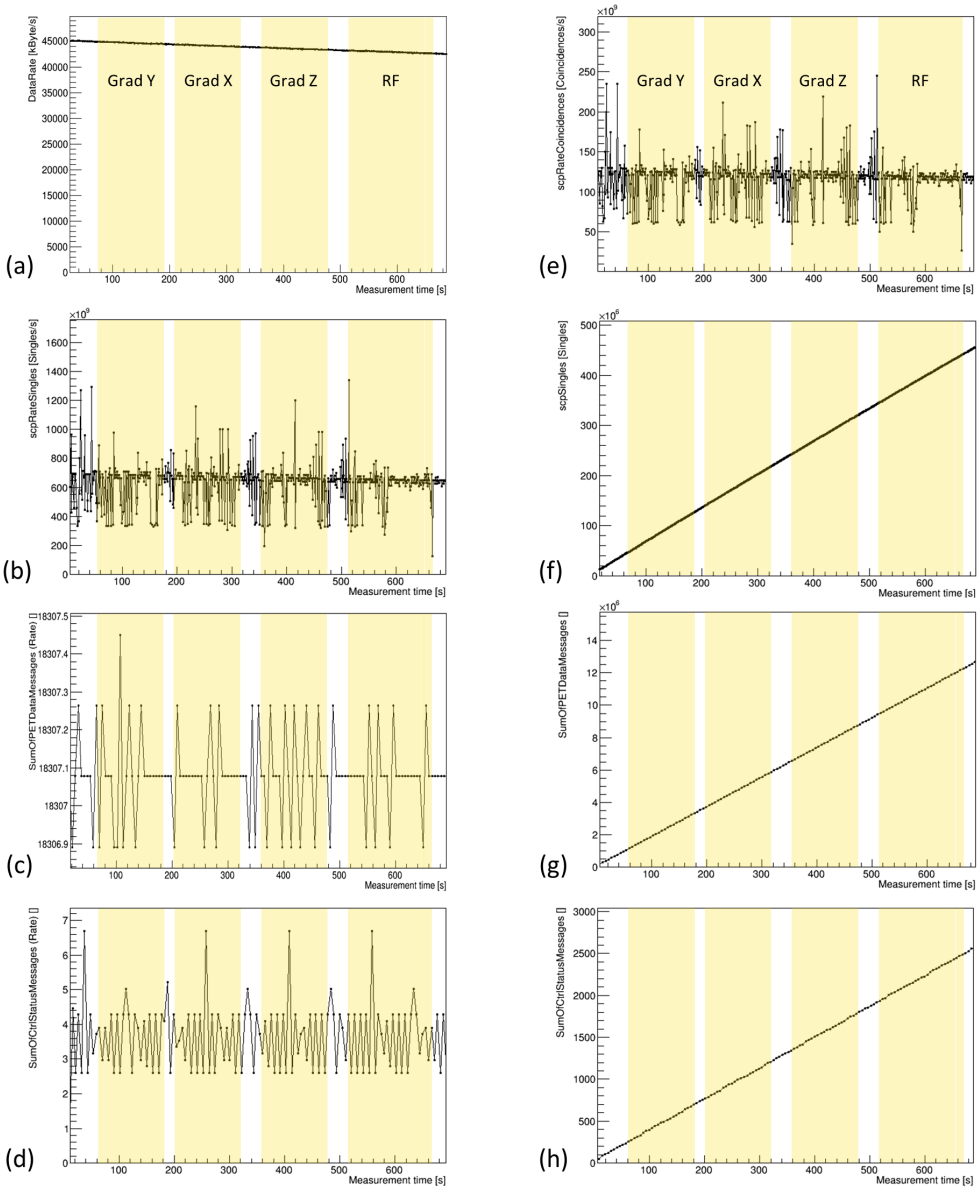


Figure 3.23: PET/MR measurement results done for an activity range between 26.5 MBq and 24.6 MBq): (a) shows the total data rate of SDM 3,(e) the total Coincidences rate of the PET insert,(b) the total Singles rate,(f) the cumulative amount of Singles,(c) the ctrl/status data message rate of SDM 3,(g) the cumulative ctrl/status data message amount of SDM 3, (e) and (f) the PET data message rate and cumulative PET data message amount of SDM 3. The shaded areas in the plots represent time periods of MRI sequences execution.

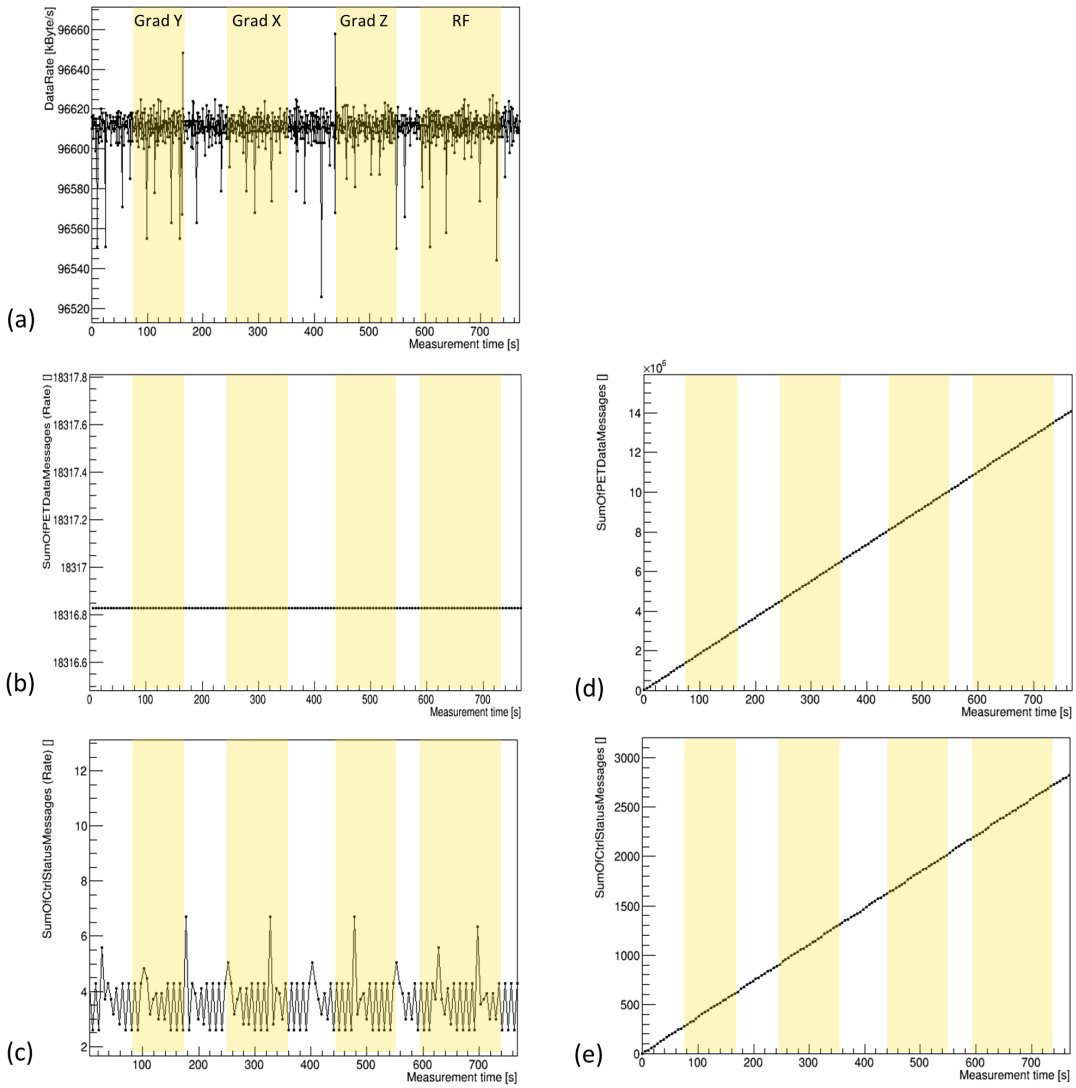


Figure 3.24: PET/MR measurement results of SDM 3 for a PET sensor data generator setting leading to the full bandwidth usage): (a) shows the total data rate of SDM 3,(b) the PET data message rate,(c) the cumulative PET data message amount,(c) the ctrl/status data message rate and (e) the cumulative ctrl/status data message amount. The shaded areas in the plots represent time periods of MRI sequences execution.

3.4 Discussion

The data-generator-based measurement results presented in figs. 3.16 and 3.17 demonstrate expected behaviour regarding the PET data message handling in

the SPU FPGA design. As soon as the bandwidth limitation of the PET data path (i.e. the path between the PET data arbiter/encoder stage and the arbiter for the shared data path) is reached, the PET data message FIFOs between the data type splitters and the arbiter/encoder inputs are not able to store a complete PET data message any more due to the congestion. In such a case, the data type splitters discard incoming PET data messages until space in the destination FIFOs is available again. Figure 3.16(d) shows that the calculated lower limit of the average PET data message transmission rate under highest data rate equally provided by all stacks matches with the measured value of approx. 4.4 PET data messages per time frame. Throughout the covered bandwidth range, no faults were detected during deactivated message sequence number tracking. The occurrence of missing messages was studied under saturation conditions in the SPU FPGA and the results were shown in fig. 3.18(d) and fig. 3.19(d). Discarded messages were tracked by the analyser and fault information was stored in its memory until the latter became full. Upon a detected fault, the analyser also stores information about the preceding message in case the latter was healthy. This serves debugging purposes and results in two memory line entries. With a memory capacity of 2048 lines, 1024 entries contain information about an actual fault, when faulty messages are not successive at the output of the second arbiter stage towards the shared data path. This corresponds to the amount of faults tracked for both measurements. The provided information about the origin of the messages that were discarded indicates an equal distribution over the six stacks to be expected using a message-based round-robin arbitration scheme. A quantitative analysis of the distribution has not, however, been performed, yet.
The ctrl/status data message rate remains constant throughout the whole measurement ranges for both environmental sensor read-out rates of 1 s and 100 ms. In the latter case, requesting a total amount of 22 ctrl/status messages per SDM over a period of approx. 305 time frames is more than enough for the second-stage-arbiter to grant the access for a ctrl/status message to the shared data path between two PET data messages. With a ctrl/status message FIFO size of 2048 bytes between the ctrl/status data arbiter/encoder stage and the second-stage arbiter towards the shared data path, temporary storage is sufficient even for a high amount of small ctrl/status messages or a few larger ones in case of a sustained high transmission load along the PET data path towards the shared path.

The measurements with ^{18}F confirm the message transmission behaviour observed for the data-generator-based measurements. Unfortunately, the software-based data acquisition was interrupted for a time window of 36 minutes between the a isotope activity of 47.8 and 38.1 MBq due to an unexpected shut-down of the software running on the acquisition server. The first measurement set, however, was acquired during an activity range which resulted in a bandwidth saturation in all SDMs. The results shown for SDM 3 in fig. 3.20 visualise the average PET data message rate increase with decreasing activity until the SDM leaves saturation in the SPU FPGA which results in a constant rate, while the ctrl/status message rate remains constant over the entire measurement time. Figure 3.20(e) visualises tracked header-CRC faults spread over a time range of approx. 19 minutes which occur in seven periods with time periods between them without any header-CRC faults. The tracking stopped when the memory was full. The fault amount is very low compared to the difference in orders of magnitude regarding the sum of PET data messages verified by the analyser (over 30×10^6 PET data messages), but was also detected within other SDMs during the measurement. This needs further investigation. Messages with a detected invalid header CRC are discarded from the data stream by the splitters and thus not analysed any more regarding their payload. The splitter afterwards looks for a preamble of a new message.
Similar to the data-generator-based measurements, the sequence number tracking for PET data messages was disabled to allow for tracking of other fault types when acquiring data during saturation. However, if other fault types would also be detected repeatedly, the memory could fill up before the measurement end would be reached. Here, an improvement would be to use the external DDR2-memory as a large buffer and to automatically transmit the analyser's local memory content upon a threshold crossing to the external DDR2-memory. This could greatly extend the measurement time during which detected faults could be stored and read out after completion of a measurement. The latter would avoid distortions of the actual measurement conditions due to a high ctrl/status data message transfer which otherwise would not appear during a PET data acquisition.
The average PET data message rate per time frame as shown in fig. 3.21 reveals that the message rate measured at 85 MBq for the chosen DPC sensor settings is approx. 0.8 messages per time frame away from the lowest limit of 4.4. These means that the PDPC processing chains in the Stack FPGAs where not in sat-

uration (when averaged over all 16 DPC sensor input channels), yet.
During the second measurement period covering 38.1 down to 2.4 MBq, no faults were detected by the message analyser. For this period, the missing-sequence-number tracking was activated and the message statistics counter reset. In fig. 3.20 (b) and (d) are clearly distinguishable a lack of transmitted information from the acquisition server to the control PC. It is not known, what prevented the server on the acquisition server side during a period of over 23 minutes from a flawless operation. The SDMs operated without problems during this time which can be determined by the linearly increasing sum of data messages shown in figure (f) and (g). However, the fluctuations of the PET message rate shown in figures (c) and (e) need to be analysed in the scope of future studies. The same applies to the acquisition interruption which occurred during the execution of the online-software processing software on the server. In the past, measurements with online-data-processing over longer periods of time as presented in [158] were, however, not done continuously, but divided in several measurements followed by linux-based cache memory flushing prior to a new measurement. In [158], the data quality of messages from the PET insert received by the acquisition server was analysed for the same DPC sensor settings as used for the ^{18}F measurements presented in this chapter. Although it was determined that 99.99 % of received bytes were valid [158], it remained unclear, if data corruption appearing within the bandwidth range of the SDMs occurs within the SDMs themselves or during UDP transmission towards the server. In order to answer this open question, further investigations are needed. The memory depth for the message analysers needs to be extended and the PET measurements in the bandwidth range for a tracer activity greater than 38 MBq for the given sensor settings need to be repeated. The results obtained with the FPGA-based analysers then need to be compared to a data integrity analysis of the messages acquired at the software side (DAPS).
The PET/MR measurements revealed that gradient field switching with strong slew rates as well as RF field excitation do not impair the digital data transmission within the SDMs. Particularly the transmission between the stack and SPU FPGAs was given attention by verifying not only the header- but also the payload-CRC of the data messages in downstream direction in order to identify bit-flips as a result of signal induction along the electrical transmission lines.

The data transport can therefore be considered to be stable during simultaneous PET/MRI operation.
Regarding the current bandwidth limitation as such, the throughput of the SPU FPGA design could be increased by adjusting the clock frequency for downstream-data-path-related FPGA logic. By doing so, the bandwidth can be adjusted to the one of the GBitE module which would then become the bottleneck of the SDM's data path. A big improvement for PET imaging would be obtained by performing on-line processing of the raw detector (hit) data to form singles. The FPGA implementation is prepared for an integration of processing pipelines and FPGA-based data processing is planned as the next step to increase the imaging capabilities at high count rates for this and future systems. Provided that Singles processing would be done by SDMs during data acquisition, FPGA-based online coincidence processing could be considered, too. As an alternative to a central coincidence processing node, daisy-chain-based coincidence processing could be explored by using the SDMs with removed RF shields. Their PCB design include the connection of a second optical link to be used between SPUs allowing to search for coincident Singles via the daisy-chain. Additionally, sufficient FPGA logic resources need to be available in order to implement the search for coincident events in parallel to singles processing.
Some improvements related to the transmission behaviour of the system are also subject to future works. Currently, the second arbiter stage lacks an algorithm allowing ctrl/status data messages to be favoured over PET data messages when the shared data path approaches its throughput limitation. As introduced in section 3.2, this would maintain under any ratio of ctrl/status to PET data message rates the full monitoring and control capabilities of a PET system. High amounts of ctrl/status data during a PET data acquisition could arise when the system is driven in saturation while control- or configuration-related procedures take place. Albeit the lack of prioritisation implementation is not an issue with the current implementation for Hyperion II$^{\mathrm{D}}$ when performing PET scans within the available bandwidth, this improvement is subject to future acquisition-platform-related works, as an improvement of the system is ongoing with respect to the two Hyperion II$^{\mathrm{D}}$ prototypes being used for research in the field of PET/MR instrumentation as well as imaging applications.
The big difference in message size between ctrl/status messages listed in table 3.3

and large PET data message sizes occurring under high count rates decreases the fairness with regard to shared bandwidth of the common data path particularly for the case of message-based arbitration scheduling. With the simple Round-Robin scheme applied by the second arbiter stage, ctrl/status messages suffer from a low bandwidth access compared to large PET data messages. This could be improved with the Weighted Round-Robin scheme [161], where weights can be assigned to requesters. This would allow the transmission of more than one message from the non-empty ctrl/status data FIFO before messages from the PET data FIFO would be forwarded by the second-stage arbiter. Weighted round-robin is message-based and thus does not consider the difference in message sizes. A large variation in size would still have a negative impact on the resulting fraction of bandwidth to be shared by ctrl/status and PET data messages. Therefore, the (Weighted) Deficit Round-Robin (DRR) arbitration [162] scheme would be of interest, as it decreases the inequality in fractional bandwidth usage for messages of different sizes by taking the message size into consideration during scheduling. However, considering the low ctrl/status data message rate used during PET data acquisition even under high rates in case of Hyperion II^D, ctrl/status message would not benefit from DRR in order to increase the average fractional bandwidth allocation.

In order to further test the data transmission behaviour of the FPGA-based platform regarding the current, but also for the above-suggested improvements, the data generators provided by PDPC should be optimised with regard to the choice and amount of input data per time frame. To reflect a more realistic data acquisition pattern, messaging originating from one to several DPC sensors at a same time should be generated to represent a Hit cluster triggered by a scintillation event. The amount of messages should vary per time frame to represent an actual messaging behaviour related to a gamma scintillation interaction distribution. Data generators providing synthetic and known data are an important step after successful simulations of the acquisition platform for validation purposes of the latter. However, given the complexity of such an acquisition platform, PET-tracer-triggered measurements including the PET sensor as part of the data acquisition chain remain an essential step in evaluating the entire data chain under real measurement conditions as demonstrated with the presented measurements.

3.5 Conclusion

The advancements in detector technology during the last decade from PMTs towards semiconductor-based detectors for PET offer higher system integration possibilities and enable operation of PET detectors within an MRI gantry for simultaneous PET/MR imaging. However, the usually higher fraction of detector channels per detector area for APDs or SiPMs compared to PMTs leads to an increase in detector data channels which need to be read and processed by the underlying data acquisition system. The compact sizes of FPGAs compared to their increasing logic resources make them highly attractive for PET detector data acquisition and processing using parallel and in-the-field reconfigurable data processing in PET/CT and PET/MR systems. Driven by the continuous research and development of semiconductor-based sensors on one hand and their use for a wide range of current and future PET/CT and PET/MR applications in mind, a one-fits-all approach for a PET data-acquisition-and-control architecture was presented in this chapter.

First, general architectural concepts where presented which satisfy the needs for the aforementioned requirements, covering aspects such as topological flexibilities, communication protocol, scalability, modularity, data transmission robustness and quality of service. Afterwards, the requirements for these aspects were presented with regard to the Hyperion II^D PET insert, followed by the introduction to the FPGA-based implementation of the acquisition architecture approach. In order to study the data message transmission behaviour of the implemented FPGA-based acquisition platform, data message analysers were implemented in the FPGA designs which validate the integrity of messages prior to be sent via GbitE-links to the data acquisition server. PET data measurements using data generators to trigger synthetic data as well as ^{18}F were conducted over the entire bandwidth of the SDMs and under varying messaging conditions to study the data message transmission with respect to faults or missing messages at SDM level. The measurements confirmed the calculated PET data message rejection rates when the SDMs are driven in saturation up to the limitation of the PDPC processing chains. The ^{18}F measurement revealed header-CRC faults for tracer activities beyond 70 MBq detected by message analysers within the SDMs. Further investigations are necessary to identify the faults' origin at the data type

splitters. However, this did not have an impact on the stability of the data transmission. No data message faults were detected along the shared downstream data path in the SPU FPGA design for an activity range between 38.1 MBq and 2.4 MBq. Finally, simultaneous PET/MRI measurements were performed in order to analyse, if data integrity is impaired in the SDMs when MR sequences generating gradient field switching at high slew rates and repetitive RF field excitation where executed. No faults were detected during MRI sequence execution, demonstrating the strong magnetic as well as electromagnetic fields do not corrupt the digital data transmission of the Hyperion II^D.

Chapter 4

RESCUE - Reduction of MR SNR degradation by using an MR-synchronous Low-interference PET acquisition technique

4.1 Introduction

When PET detectors with electronic circuits are located within or in close proximity to the MRI bore, RF fields originating from the RF coil during the MRI RF excitation phase and from the PET-electronics degrade the performance of the PET and MRI subsystems, respectively. As introduced in section 2.4.1, RF shielding of the PET detectors is therefore commonly applied to overcome this RF-interference-related issue.

To shield PET detectors so as to avoid mutual interferences between PET and MRI subsystems, academic research groups and companies have explored different material types, thicknesses and structures for RF shields. Materials to be used for EMI shielding are amongst others distinguished by their conductor properties. Copper has been mainly explored and used for PET detector RF shielding [117, 103, 101, 100, 102, 86, 112, 163, 164, 165, 135, 124, 111, 106], followed by

gold [118, 163], aluminium [111, 109] and carbon fibre [125, 149]. Investigations using segmented structures for the shielding material have yielded a reduction of eddy current loops when compared to unstructured, continuous material surfaces as reported in [141, 111] and were also used by [165, 163].

As EM field shielding requires the use of conductive materials, eddy currents are generated inside the shields when the latter are exposed to time-varying magnetic and EM fields as is the case for MRI-related gradient and RF fields (see section 2.4.1). These eddy currents create local opposing magnetic fields, leading to MRI B_0 and gradient field disturbances close to the shields. In addition to segmented structures, a possibility to reduce eddy currents is to thin down the material layer thickness. However, this reduces the RF attenuation capability, as the thickness determines the RF field attenuation strength, being the primary purpose of the PET detector shielding. Therefore, the shielding material structure and thickness design is a trade-off between satisfactory RF shielding on one hand and minimised, eddy-current-related local magnetic field disturbances on the other hand. As the shield does not entirely enclose a PET detector for practical reasons of cabling and cooling tube lead-throughs, RF field leakage (as reported in [117]) of fields originating from PET electronics as well as the MRI may occur [166], leading to impaired PET and MRI performance when not carefully taken into account during the design and assembly process. Another downside associated with the use of RF shielding is an increased B_0 distortion related to susceptibility shifts which are caused by the shield materials when placed into the MRI bore FoV.

The above-mentioned shield-related disadvantages, which can degrade the MRI image quality, could be entirely avoided, if PET detectors could operate within the MRI without RF shielding at all while demonstrating an unaffected PET performance during simultaneous operation. PET detectors with no need for RF shielding could offer new possibilities in terms of a higher integration within the MRI subsystem in order to maximise the FoV shared by PET and MRI in transaxial direction. However, omitting shielding would also require the RF fields emitted by the PET subsystem to couple as little as possible into the MRI RF receive coil during MR image acquisition to preserve the MRI SNR.

Regardless of whether a PET subsystem is designed with or without shielding, the MRI SNR performance of a hybrid system might be considered unsatisfactory

for particular PET/MR imaging protocols when demanding MRI sequences are used, even though the system performs well for a wide range of other imaging applications and protocols. Typically in MR imaging, high-resolution scans and fast-imaging protocols are very susceptible to low SNR which is due to the trade-off between SNR and image resolution or scan time. Hence, the preservation of the intrinsic MRI performance during the application of such MRI sequences (commonly used in Cardiovascular MR imaging (CMR) and preclinical high-resolution imaging) is of highest interest to detect very small MRI signals.
This chapter presents a gating-based method for hybrid PET/MRI configurations which aims at the aforementioned MRI SNR preservation by MR-synchronously interrupting the data acquisition of the PET subsystem during MR RF signal receive phases. The interruption allows the reduction of the noise picked up by the MRI which is related to RF field emission being caused by data acquisition electronics during PET data acquisition (see section 2.4.3). As the name of the technique suggests, RESCUE as a gating method aims to expand the range of MRI-SNR-critical PET/MRI protocols with satisfactory MR imaging results by preserving the MRI SNR performance using PET data acquisition gating. When compared to gating methods reported in literature, PET data acquisition gating techniques have previously been proposed to correct and improve motion-related or MRI-RF-excitation-related PET image artefacts [106, 167, 74], but not for MR image quality preservation.
The concept of RESCUE can be applied to the Hyperion II^D PET insert by interrupting the DACA using MRI trigger signals which may either be provided by the MRI system or via the Rx/Tx RF coil. In order to interrupt (stop) and release (start) the data acquisition of the Hyperion II^D DACA to perform PET data acquisition between consecutive MRI RF receive phases being typically in the range of single-digit milliseconds, a new method was developed and implemented in firmware to quick-stop and -start the DPC sensors with latencies much lower than the conventional DPC sensor start/stop procedure. This new quick-start/stop method for the DPC sensors is introduced in addition to the methodology of RESCUE in this chapter, followed by MRI SNR and noise measurement methods as well as their results using a single SDM to investigate the RF noise reduction obtained with RESCUE. Finally, the impact of the MRI RF acquisition duty cycle on the PET data acquisition interruption duty cycle

are discussed for exemplary chosen, common MRI sequence types to illustrate that the suitability of RESCUE is dependent on the aimed PET/MRI protocol.

4.2 Methods

4.2.1 DACA requirements

In order to determine timing-related requirements for the PET subsystem to be interrupted regarding its data acquisition for time periods in the range of the MRI RF acquisition cycles, an example MRI sequence was used to define PET-related timing parameters. Afterwards, their values were calculated for a set of typical MRI sequences and the requirements derived from that.
The upper part of the timing diagram shown in fig. 4.1 represents an MRI spin echo sequence (simplified with focus on RF, only) with a duration defined by the repetition time T_R. During the time T_A^{MRI}, the MRI acquires the RF signal generated by the nuclei relaxation period.

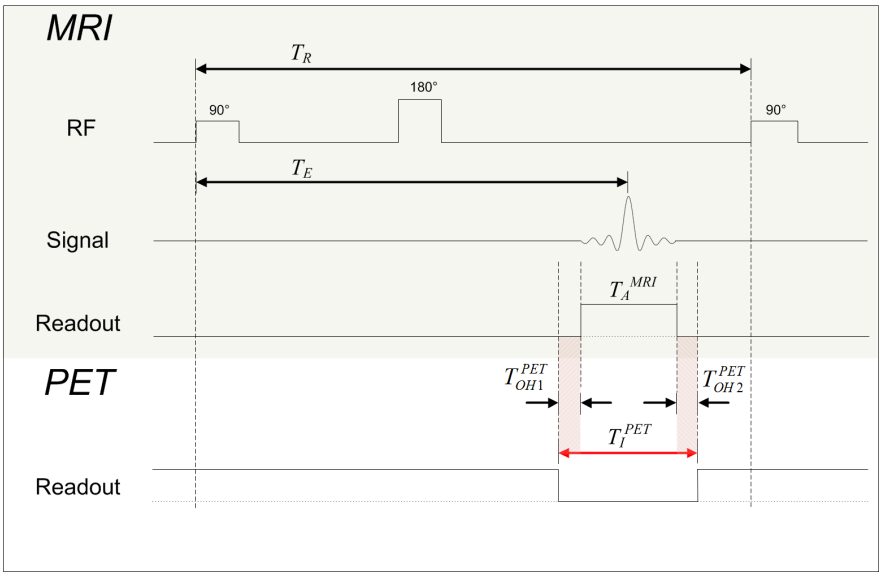


Figure 4.1: Simplified timing diagram of an MRI spin echo sequence with repetition period T_R and the MRI RF acquisition performed after proton echo generation phase T_E. A PET data interruption period T_I^{PET} is to be executed during RF acquisition time T_A^{MRI} with T_I^{PET} close to T_A^{MRI} to keep overall PET sensitivity loss low.

To reduce PET-related RF field coupling into the MRI RF coil during T_A^{MRI}, the PET data acquisition of the PET detectors shall be interrupted for the time T_I^{PET}, with

$$T_I^{\mathrm{PET}} \geq T_A^{\mathrm{MRI}} \tag{4.1}$$

As the data acquisition interruption will introduce a PET sensitivity loss, the time window T_I^{PET} should be as close as possible to T_A^{MRI}. An overhead being the time difference between T_I^{PET} and T_A^{MRI} may technically occur and shall be defined as the overhead time T_{OH}^{PET}. It is on one hand composed by the overhead time T_{OH1}^{PET} occurring between the interruption of the PET data acquisition and the actual begin of the MRI acquisition phase and on the other hand consists of the overhead time T_{OH2}^{PET} covering the period between end of the MRI acquisition phase and the release of the PET data acquisition interruption. This is depicted in fig. 4.1 and summarised by eq. (4.2):

$$T_I^{\mathrm{PET}} - T_A^{\mathrm{MRI}} = T_{OH}^{\mathrm{PET}} = T_{OH1}^{\mathrm{PET}} + T_{OH2}^{\mathrm{PET}} \tag{4.2}$$

The entire amount of MRI acquisition phases T_A^{MRI} during a single T_R equals $TF * T_A^{\mathrm{MRI}}$ with TF being the Turbo Factor of a given MR sequence:

$$\sum T_A^{\mathrm{MRI}} = TF * T_A^{\mathrm{MRI}} \tag{4.3}$$

Using this, an MRI RF signal acquisition duty cycle DC_A^{MRI} can be defined as the ratio of all MRI acquisition phases T_A^{MRI} occuring during one T_R, and T_R itself:

$$DC_A^{\mathrm{MRI}} = \frac{\sum T_A^{\mathrm{MRI}}}{T_R} \tag{4.4}$$

A measure for the PET data acquisition interruption duty cycle can be defined similarly to eq. (4.4):

$$DC_I^{\mathrm{PET}} = \frac{\sum T_I^{\mathrm{PET}}}{T_R} \tag{4.5}$$

Depending on how large the fraction T_{OH}^{PET} of T_I^{PET} is compared to T_A^{MRI}, DC_I^{PET} may increase undesirably depending on TF. Generally, the smaller the

Table 4.1: Set of commonly used MRI sequences with some used to evaluate the PET insert *Hyperion I*. (© 2015 IEEE. Reprinted, with permission, from [49]).

MRI sequence name	$\frac{T_R}{ms}$	$\frac{T_E}{ms}$	$\frac{T_A^{\mathrm{MRI}}}{ms}$	TF	$\sum \frac{T_A^{\mathrm{MRI}}}{ms}$	$\frac{DC_A^{\mathrm{MRI}}}{\%}$
T1W_aTSE	612	20	3.81	6	22.83	3.72
T2W_TSE	2400	100	3.81	16	60.96	2.54
T1W_3D_FFE	11	2.3	1.62	1	1.62	14.73
T2W_3D_FFE	13	8.1	4.62	1	4.62	35.54
EPI_7	43	20	3.80	7	26.60	61.86
Brain-T1W-FFE	25	1.85	3.27	1	3.27	13.06

PET data acquisition interruption $\sum T_I^{\mathrm{PET}}$ can be kept, the higher the resulting PET sensitivity during simultaneous PET/MRI operation using RESCUE.
To determine an order of magnitude as a requirement for T_{OH}^{PET}, some commonly used MRI sequences listed in table 4.1 with parameters T_E, T_E, T_A^{MRI}, TF and parameters introduced in eqs. (4.3) to (4.4) are shown for comparison purposes.

Turbo-Spin-Echo (TSE) sequences have a low MRI duty cycle (i.e. as defined above), whereas Echo-Planar-Imaging (EPI) sequences always have high acquisition cycles. As an example for a sequence type with duty cycles being in between those of the aforementioned TSE and EPI sequences, T_2-weighted Fast-Field-Echo (FFE) sequences typically have repetition times in the range of 10 to 50 ms. With an acquisition period of 13 ms for the particular T2W_3D_FFE sequence depicted in table 4.1, DC_A^{MRI} equals 35.54 %. If one aims to avoid PET data acquisition interruption duty cycles $\geq 50\,\%$, then the total overhead time T_{OH}^{PET} should not exceed 1.88 ms. Thus, it is favourable to keep PET interruption overhead times below 1 ms to reduce the overhead-time-related impact on PET sensitivity for a range of MRI sequences with higher MRI signal acquisition cycles while avoiding DC_I^{PET} to exceed 50 %. In case of the T2W_3D_FFE sequence, an interruption overhead time of 1 ms would contribute 21.6 % to an overall PET sensitivity loss resulting with $\sum T_I^{\mathrm{PET}} = 5.62$ ms.

4.2.2 Conventional start/stop of the DPC sensor operation

The configuration of the DPC sensor is performed using the JTAG interface (see section 2.1.2.4). Configuration data includes parameters such as validation times and schemes, trigger schemes, inhibit memory content as well as control bits to start or stop the main acquisition and pixel controllers [168]. To successfully configure the DPC sensor prior to data acquisition start, PDPC advises to perform the following consecutive steps using JTAG:

1. Initiate a JTAG reset command to set JTAG controller of the sensor, main acquisition and pixel controllers to *idle*-states, and time stampers to zero.
2. Program the inhibit memory to switch off SPADs with dark-count rates considered too high.
3. Set parameters such as validation times and schemes, trigger settings and integration time.
4. Initiate another JTAG reset to move aforementioned controllers to *idle*-states.

The DPC sensor is now ready for data acquisition by applying the sensor die clock signal. To stop a running acquisition, the following procedure is advices by PDPC (Philips Digital Photon Counting, Aachen, Germany):

1. The main acquisition controller's activity needs to be stopped by forcing the controller's two FSMs to remain in their *idle*-states. This ends the data acquisition in a controlled way while the sensor die clock is still active and is achieved by programming the JTAG configuration register.
2. Program the inhibit memory to deactivate all SPADs of the DPC sensor to avoid any further SPAD breakdown and recharge.
3. Apply a JTAG reset.
4. Deactivate the sensor die clock signal.

The DPC sensor data acquisition termination procedure ensures that the acquisition controller's event acquisition finite state machine (FSM) is not in *diode-recharge* state while deactivating the sensor die clock. This is important in order to avoid the SPADs drawing recharge currents longer than specified (recharge time range: $10 - 40\,\text{ns}$ [168]). Doing so prevents a heat-up of the SPADs which leads to SiPM gain variations. Furthermore, depending on the recharge voltage supply design, a supply overload may occur.
Both the acquisition start and stop procedures include an inhibit memory program step which covers most of the procedures' time. In the case of the sensor tile used for Hyperion II$^{\text{D}}$ with 16 sensor dies per JTAG chain (see section 3.2.3.1 (paragraph *dSiPM sensors*), 11.85 ms are needed to program the inhibit memories assuming that the maximum JTAG clock frequency of 50 MHz is applied. As a comparison, the time needed to program configuration parameters via JTAG at the same JTAG frequency takes $238\,\mu\text{s}$, which is 50 times quicker. Summarised, the total time needed to start and stop the DPC sensor's data aquisition does not allow the total PET data acquisition interruption overhead time to be met for a start and stop procedure of 1 ms or less as determined as a requirement in section 4.2.1.

4.2.3 Quick DPC sensor operation interruption

To still be able to use the DPC sensor for RESCUE while fulfilling the timing requirement for T_{OH}^{PET} as well as the SPAD-recharge timing specifications, an alternative start/stop approach was developed. It is based on interaction between the DACA and individual DPC sensors, prior knowledge of the DPC sensor's FSM design, and based on the fact the sensors' FSMs behave deterministically in time while being synchronously clocked with the stack FPGA.
Figure 4.2 shows a combined diagram of the two FSMs in the DPC acquisition controller showing their states, the state residing times as well as transitions and transition conditions, if existing. The diagram was simplified by grouping states with same overall functionality to single ones.

After a succesfully validated trigger (section 2.1.2.4), the event acquisition FSM transitions through photon counting (*collection*) and *readout* states before

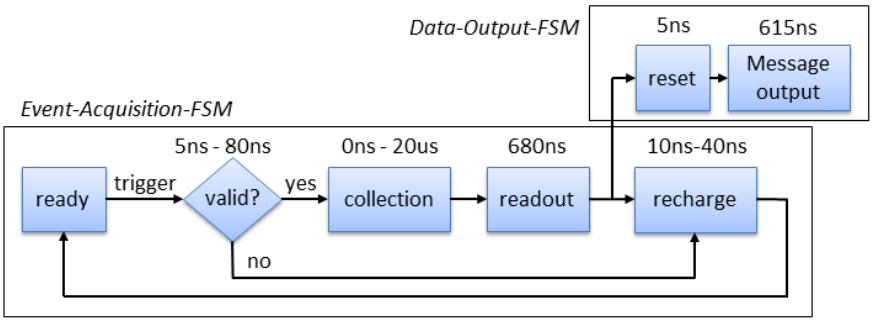


Figure 4.2: State machine states and transitions of the two FSMs within the DPC sensor acquisition controller (© 2015 IEEE. Reprinted, with permission, from [49])).

it unconditionally enters the *recharge* state and at the same time triggers the data output FSM to generate a new data message. Due to fixed message output length and the unconditioned triggering of the data output FSM taking place at the same point in time as when the *recharge* state is entered by the acquisition FSM, one can determine a point in time at which it is safe to deactivate the sensor die clock while the acquisition FSM is not in *recharge* state. The need for a new message to be detected by the stack FPGA, however, implies that one would need to wait for a successfully validated event for the acquisition controller to initiate a message generation. This adds unpredictable delays between the beginning of a clock interruption procedure and a subsequent message detection on the way to the aimed clock signal interruption. Therefore, an external trigger signal is applied to the sensor die which forces a successful trigger validation (section 2.1.2.4) to generate a new data message. While an external trigger signal is applied, the acquisition controller might be in the process of transmitting a data message which was triggered by a scintillation event (i.e. not triggered via external trigger input). Then, an additional delay adds to the total latency between the beginning of the clock interruption procedure and the actual clock interruption. In the worst case, the DPC sensor data message start bit is missed by the FPGA at the clock cycle at which it becomes sensitive to it for the purpose of an interruption procedure. Here, one would need to wait for the remaining bits of the message to be read before the externally triggered one can be detected, thereby adding to the total latency an additional delay between the evaluation of the external trigger by the event acquisition FSM and the detection of a new

message. While the DPC sensor acquisition controller is processing a triggered event, it will not recognise the externally applied trigger as the latter is not latched. Thus, the stack FPGA needs to keep the external trigger active until a new data message is detected.
After a clock signal interruption, an interruption release can be applied at any point in time with the DPC sensor being ready for data acquisition upon clock reactivation without any need for further JTAG-configuration-related considerations.

4.2.4 Operation of RESCUE

One full operation cycle of RESCUE can be logically divided into three states:

- State 1: The MRI-triggered PET data acquisition interruption procedure to be completed before the MRI enters the actual MRI RF acquisition phase.
- State 2: The PET data acquisition being stopped while the MRI acquires RF signaling.
- State 3: The MRI-triggered release of the interruption to be issued after completion of the MRI signal acquisition.

These states are described in more detail below for an implementation using the Hyperion II^D platform.
The layout of the triggering and its propagation between the MRI and the PET subsystems comprises equipment located in the MRI technical and examination rooms as depicted in fig. 4.3. An MRI trigger may be provided in two different ways: Either by the MRI processing system or by the splitter box electronics provided with the MRI RF Tx/Rx coil. When MRI processing-electronics-based triggering shall be used, a TTL trigger signal must be provided to the Hyperion II^D remote trigger unit (RTU) located in the MRI technical room which, in turn, forwards the trigger optically to the CSU. In case of triggering provided via the RF coil electronics, an optical signal is directly sent to the CSU. From there on, the CSU FPGA generates a *gate* signal which is distributed to all SDMs of the PET subsystem via the dedicated optical fibres also used for synchronisation pulse and reference clock (refCLK) transmission. Each SPU FPGA of an SDM

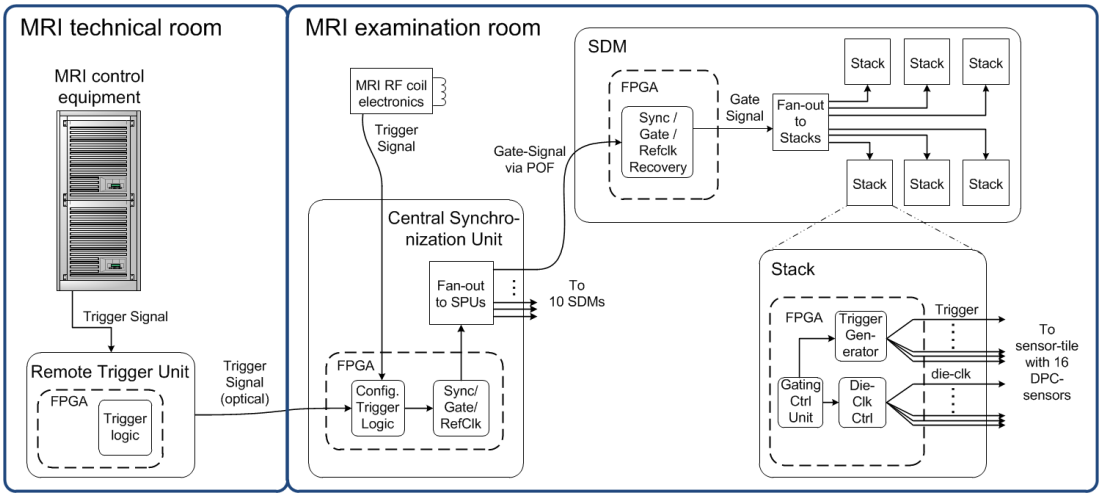


Figure 4.3: Block diagram of the trigger signaling path between the MRI and PET subsystems (© 2015 IEEE. Reprinted, with permission, from [49]).

recovers the gate pulse from the combined sync/gate/RefCLK signaling and forwards it to all stack FPGAs via the SPU fan-out chip. A firmware design unit that controls the DPC sensor triggering upon gate pulse detection will then raise external trigger signals to all sensor dies of a sensor tile via dedicated trigger lines (see fig. 3.8). At this point, the interaction between the sensor dies and the FPGA occurs at DPC sensor level, as sensor data messages are sent individually upon sensor triggering, requiring the FPGA logic to interact with each sensor separately in terms of external trigger handling, message start bit detection and sensor die clock signal interruption. This means that the clock signals of the 16 sensor dies on a tile may be interrupted at different point in times, as the trigger signals might be activated while some of the sensor dies transmit a data message originating from a scintillation event to the FPGA whereas others dies don't. Therefore, the PET data acquisition is considered entirely interrupted only when the last of all sensor dies gets its clock signal deactivated. In fig. 4.4, a timing diagram visualises and summarises the course of actions with a focus on the interaction between the FPGA logic and one sensor die. T_{OH1} begins with the last sensor die clock signal interrupted, when considering more than one sensor die.

While the PET data acquisition is interrupted (RESCUE - state 2), the PET-DACA-wide time frame counting remains ongoing. This is important in order to keep consistent and continuous the global PET time stamping over the duration

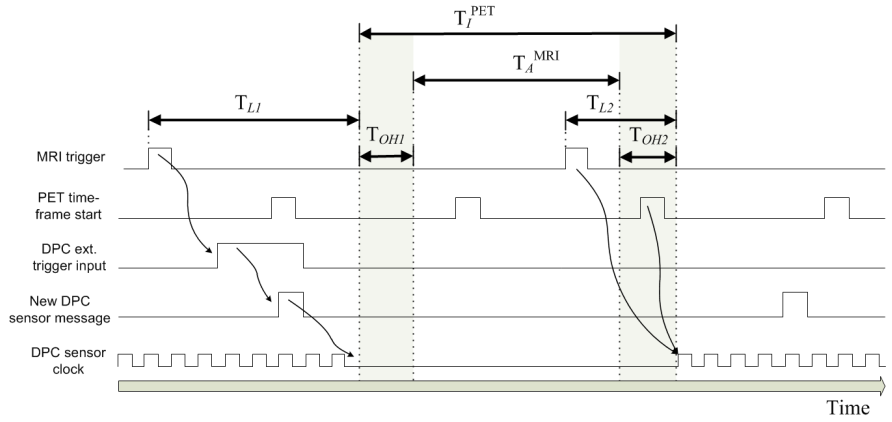


Figure 4.4: Simplified timing diagram for RESCUE focusing on the interaction between a stack FPGA and one sensor die: An MRI trigger is generated and forwarded to the stack FPGA which, in turn, raises a external trigger to the sensor die to force a data message generation. The sensor die clock is switched off after a message start bit detection at a point in time where SPADs are not recharged (© 2015 IEEE. Reprinted and adapted, with permission, from [49]).

of a complete PET/MR imaging protocol regardless of applied gating techniques such as RESCUE. Ctrl/status-related DACA information might need to be time-stamped or frame counter values stored to be evaluated for later post-processing purposes such as gated PET imaging or time alignment for PET and MRI synchronisation purposes as done in [125, 160].

To release the PET data acquisition interruption (RESCUE - state 3), a further MRI trigger is initiated. As the FPGA-internal frame and coarse counters run continuously compared to those of the DPC sensors during deactivated clocking, the DPC sensor counters need to be realigned with the FPGA counters of the DACA. This can be achieved by storing each of the sensor die coarse counter values at the moment when the DPC sensors' clock signal is deactivated. During the interruption release procedure, the clock is then applied as soon as the stored coarse counter value matches the one of the FPGA coarse counter so that these are realigned. A drawback of this solution is the higher amount of FPGA logic resources needed for 16 comparators and logic to individually apply the sensor die clock signals. Another possibility to release the interruption with aligned counters is to initiate a JTAG reset of all sensor dies to reset their coarse counters while their data acquisition is interrupted (state 2) and wait for a new PET-system-wide time frame after the interruption release procedure was initiated. Once a

new time frame is detected, the sensor die clock is activated for all sensor dies (see fig. 4.4). The PET data acquisition is now resumed, a RESCUE operation cycle is completed and the PET subsystem ready for a next MRI-triggered data acquisition interruption.
Both the procedures to introduce and release the data acquisition interruption need to be initiated with lead times derived from the sum of latencies occuring between the MRI-triggering and the actual PET-system-wide data acquisition stop and start. When MRI-RF-coil-driven triggering shall be used, prior knowledge on coil electronics' trigger timing is mandatory to derive the total lead times for RESCUE. In case of MRI-backend-operated triggering, latencies occuring between the initiation of a trigger by the MR sequence and the actual TTL signal generation need to be determined.

4.2.5 Measurements

To evaluate the DPC sensor quick start/stop operation and the impact of the PET data acquisition interruption during MRI RF acquisition in terms of RF noise reduction, RESCUE was implemented in firmware and software at SDM level to allow proof-of-concept measurements using a single SDM directly connected to a control-PC running Hyperion console software. FPGA-based DACA design simulation at SDM level and logic analysis of the firmware implementation during operation using Xilinx Chipscope logic analysis [169] were performed to validate functionality and determine the lead time latency parameters T_{L1} and T_{L2} (see fig. 4.4) at Stack level (T_{L1}^{Stack} and T_{L2}^{Stack}). Especially the interaction between the stack FPGA's RESCUE-related logic and the sensor dies was traced with the logic analyser to validate the operation.
Singles-rate measurements were performed to verify that the PET data acquisition resumes as expected after a data acquisition interruption release using the DPC sensor quick start/stop technique. To activate and deactivate RESCUE at SDM level via the Control-PC, the SPU FPGA firmware was extended by adding the choice of a Hyperion-software-based trigger generator in addition to the MRI subsystem as a trigger source. For all measurements, the DPC sensor operation and configuration parameters were set as follows: SPAD overvoltage: 2.5 V, SPADs with highest 20% of dark counts were deactivated, validation time:

20 ns, integration time: 85 ns. The Single-rate measurement setup consisted of an SDM with six stacks mounted on a separate gantry with the SDM connected to a Control-PC and a ^{22}Na source with an activity of 3.9 MBq placed in the iso-centre of the gantry. After a PET data acquisition start, three RESCUE operation cycles were performed with time intervals of 1 s between active and interrupted PET data acquisition. RESCUE was triggered by the SPU FPGA using Hyperion software commands. Singles clustering during post-processing of the raw detector data was performed using the Centre-of-Gravity (CoG) with adaptive corner extrapolation (COG-ACE) algorithm [35].
The influence on the PET-related RF interference using RESCUE was studied by performing MRI SNR and noise measurements with the single SDM mounted on the separate PET gantry and directly connected to a control-PC (see fig. 4.5). To generate true raw detector data, a ^{22}Na point source (1.86 MBq) was attached to the SDM. Moreover, the RF shielding of the SDM was removed for improved quantification purposes to be compared between activated and deactivated DPC sensor data acquisition.

The MRI measurements were done using a 3-T clinical MRI (Philips Achieva 3T, the Netherlands) with the mouse coil (see fig. 2.25) mounted in the PET gantry.
Spin Echo sequences (T_R/T_E = 1000/50 ms, flip angle: 90°, voxel size = $0.5 \times 0.5 \times 0.5\,\mathrm{mm}^3$, acq. matrix: 160×160, bandwidth/pixel: 212 Hz) were performed to measure the SNR by imaging transverse slices of a cylindrical MRI phantom which contained 15 ml of a $CuSO_4$ solution. Based on the SNR results, noise floor histograms were determined according to the NEMA MS1-2008, method 4 [170]. In addition to SNR measurements, noise scans were conducted to study the RF noise coupling originating from the SDM by measuring the noise signal amplitude distribution within the frequency bandwidth that the MRI RF chain is sensitive to. To cover this bandwidth of approx. 1 MHz with the centre frequency equal the Larmor frequency, five TSE sequences (T_R/T_E: 1044/256 ms, TSE turbo factor: 32, acq. matrix: 1024×1024, bandwidth per pixel: 180 Hz) with shifted centre frequencies are executed. As this MRI protocol provided by Philips typically includes an RF pulse excitation with a flip angle of 1°, the noise measurement would be influenced due to the presence of the MRI phantom used for the SNR scan. In order to avoid a displacement of the measurement setup while being able

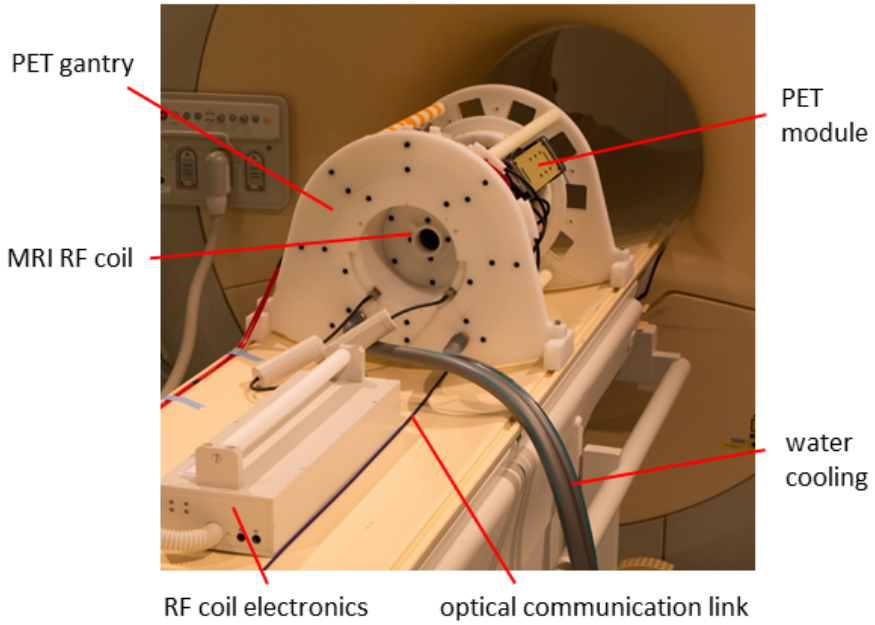


Figure 4.5: Single SDM without RF shielding. The module is mounted on the PET insert gantry with a mouse RF coil located inside (© 2015 IEEE. Reprinted, with permission, from [49]).

to do consecutive sets of SNR and noise measurements, an MRI system patch was installed with a modified MRI protocol which enabled noise scans excluding RF pulse excitations of any kind.
Three SNR/noise measurement sets where performed to evaluate the MRI RF interference impact of RESCUE: Firstly, during an ongoing PET data acquisition. Secondly, while RESCUE was active. Finally, a reference MRI scan set was acquired during which the SDM was off-powered.

4.3 Results

The maximum time between the signal assertion at the DPC sensor's external trigger input and the detection of a new message by the FPGA logic is 980 ns (at DPC sensor clock frequency of 200 MHz) when the DPC sensor is configured with the sensor configuration parameters chosen for the evaluation of the quick start/stop method. This maximum delay occurs when the FPGA message detection logic just missed the message beginning of an incoming message at the

time of the trigger-assertion. This is also the worst-case time needed until all sensor dies of a sensor tile have their clock signal interrupted. With the chosen sensor configuration parameters, the event acquisition FSM of the sensor is in *collection*-state during detection of an externally triggered new sensor message, so no SPAD recharge occurs at this point in time. Hence, the clock signal can be interrupted directly after detection of a new message.

Figures 4.6 and 4.7 depict logic analyser snapshots of signal propagations traced within the stack FPGA design to demonstrate the procedures to perform a sensor die clock interruption and an interruption release. The shown signals were chosen because of their relevance and dependencies within the clock activation and deactivation procedures to clarify and visualise the course of events. Out of the 16 available DPC sensors per tile, signals from sensors 2 and 11 were arbitrarily chosen to depict the interaction between the FPGA logic and the sensor dies. For purposes of a better overview, time periods during which no signal level changes of all shown signals took place were cropped away and are visible by dashed vertical double-lines. The horizontal axis in both diagrams represents sampling points at which signal levels were captured by the logic analyser. The sampling was synchronised to the FPGA clock frequency (100 MHz), meaning that the axis numbering is equivalent to FPGA clock cycle steps. The sensor die clock signalling could not be captured due to tool-specific constraints. Instead, the *clock enabled*-signals are shown. Both a stack-wide *enable* signal and the sensor-individual *enable* signals need to be HIGH so that the actual clock signals are forwarded via FPGA-internal clock buffers. Time marks, represented by coloured vertical lines, were used to underline important actions during the course of events.

Figure 4.6 summarises the procedure to deactivate the sensor die clocks as shown for DPC sensors 2 and 11. At time mark "T" the MRI trigger signal sent by the SPU FPGA is captured. Once detected by the stack-FPGA-internal RESCUE logic, the sensor die trigger signals are activated to initiate the data message generation. This follows the message reception (mark "O") and its detection, leading to the clock deactivation by de-asserting the *enabled* signals at mark "X" 112 clock cycles (1.12 μs) after the reception of the MRI trigger. Finally, when all individual *clock enable* signals are LOW, the signal *Stack-wide DPC sensor clocks enabled* switches to LOW, too. $T_{L1}^{\text{Stack}} = 1.12\,\mu\text{s}$ for the parameter set given

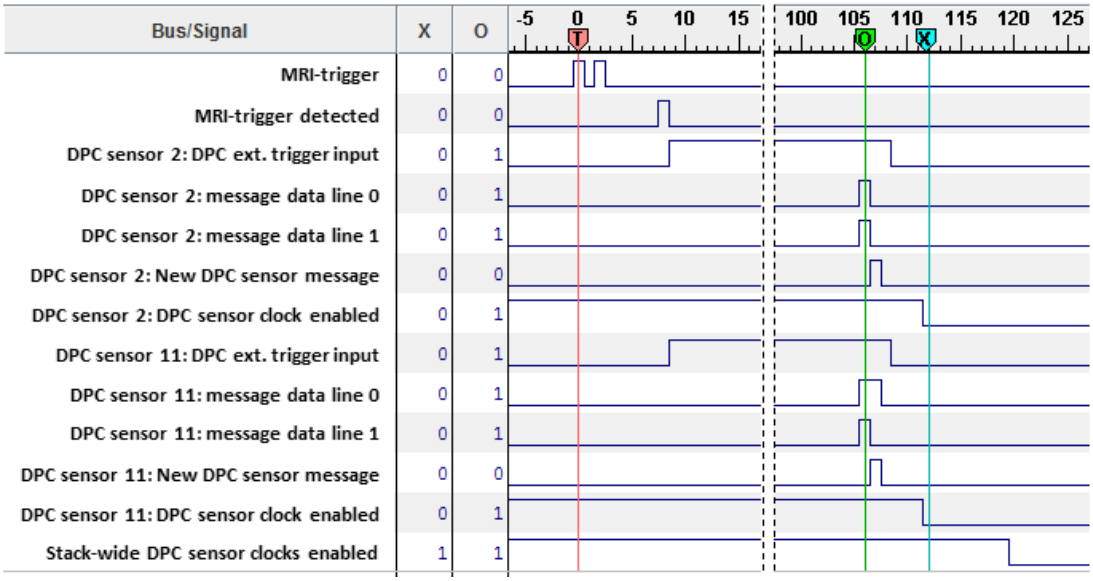


Figure 4.6: Logic analyser snapshot depicting the clock interruption procedure shown for DPC sensors 2 and 11 of a sensor tile (© 2015 IEEE. Reprinted, with permission, from [49]).

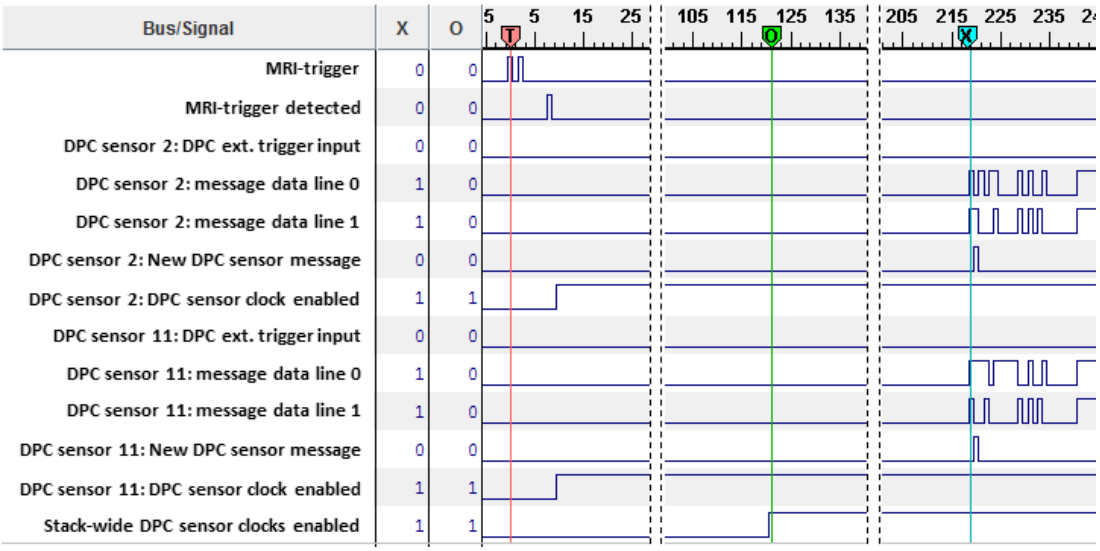


Figure 4.7: Logic analyser snapshot demonstrating the clock interruption release procedure performed on one sensor tile for DPC sensors 2 and 11 (© 2015 IEEE. Reprinted, with permission, from [49]).

in section 4.2.5.

In fig. 4.7 is shown the course of actions during the RESCUE procedure of clock interruption release to activate the sensor die clocks. After MRI trigger detection, all sensor-individual *enable* signals are asserted. The minimum lead time between the MRI trigger originating from the SPU FPGA and the RESCUE logic in the Stack FPGA waiting for a new PET time frame (frame counter increment) equals 90 ns. Once detected, the *Stack-wide DPC sensor clocks enabled* signal is activated (time mark "O") to clock all DPC sensors and resume the PET data acquisition. First DPC sensor messages after clock activation occur at time mark "X" 121 clock cycles (1.21 μs) after having received the MRI trigger from the SPU FPGA.

The Singles rate measurement obtained during a PET data acquisition that was interrupted three times using RESCUE is plotted in fig. 4.8. The RESCUE cycle time of 2 s and the interruption length of 1 s are well visible. As expected, the DPC sensor data acquisition interruption results in a Singles rate drop down to 0 cps.

The three SNR measurements obtained with the 3-T MRI are shown in fig. 4.9.

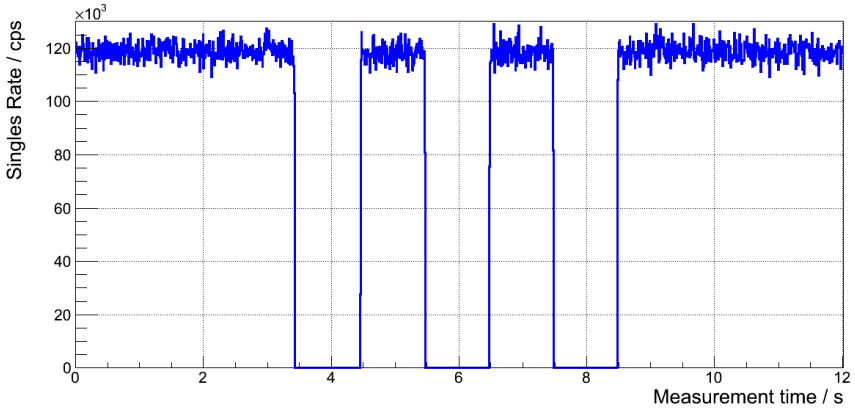
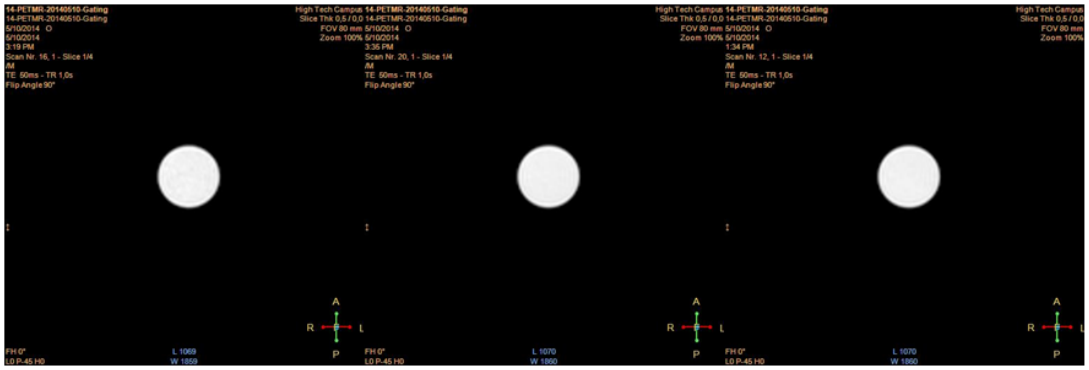


Figure 4.8: Singles rate measurement result visualising the PET data acquisition which was interrupted three times using RESCUE (© 2015 IEEE. Reprinted, with permission, from [49]).

The MRI signal pixel intensity values all are close to 68000 FPV (floating point values) in a same region of interest (ROI) for the SNR scans, meaning that changes in SNR values result from noise floor variations.

The noise floor values are depicted as histograms in fig. 4.10 together with



(a) PET DAQ active (b) PET DAQ interrupted (c) SDM off-powered

Figure 4.9: SNR measurement results: Shown is a transversal slice of the cylindrical MRI phantom used to determine MRI phantom signal intensities and background noise floor values.

Raleigh distributions fitted to the noise values of each histogram. The characteristic widths of the distributions (σ) are 738 ± 4.6 during active PET data acquisition, 380.8 ± 2.2 while the PET data acquisition is interrupted, and 378.0 ± 3.1 for the reference scan with the SDM powered off. The latter two scan results are within one standard deviation.

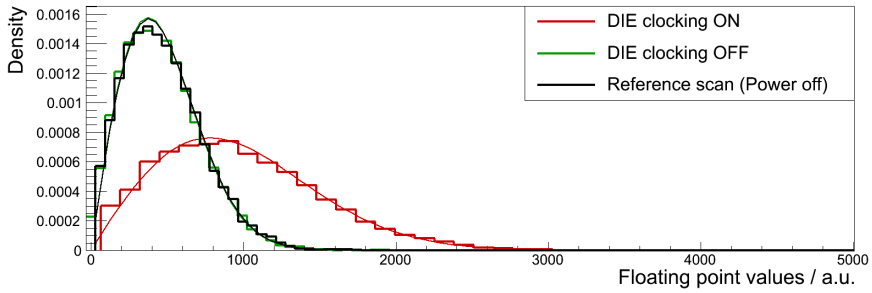


Figure 4.10: Normalised noise floor pixel histogram resulting from SNR scans during PET data acquisition (red), during PET data acquisition interruption (green), and when the SDM is powered off (black) (© 2015 IEEE. Reprinted, with permission, from [49]).

Figure 4.11 depicts the spurious noise scan results. The histogram colours were kept equal to the ones in fig. 4.10 for the three different measurements. The noise scan results confirm the noise floor measurements regarding the increased noise occurring during PET data acquisition, whereas the noise amplitude spectra obtained with activated RESCUE are comparable to those of the reference scan.

At the Larmor frequency, the PET data acquisition interruption using RESCUE led to a noise reduction by a factor of 1.9 down to the noise level of the reference scan. All noise scans reveal noise floors of broadband type which means that no noise peaks related to digital electronics were detected.

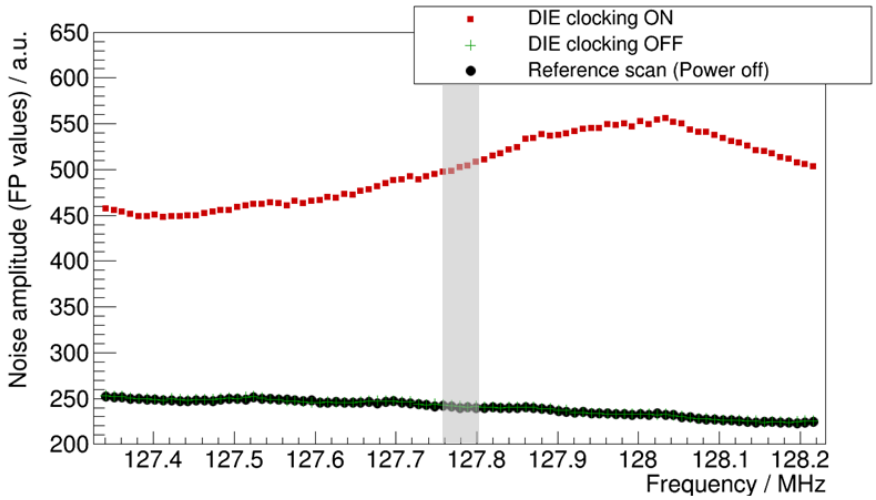


Figure 4.11: Noise scan results performed with the SDM and no RF shielding. The Larmor frequency of the used 3-T MRI being at 127.78 MHz is highlighted with a grey-shaded area (© 2015 IEEE. Reprinted, with permission, from [49]).

With the latencies determined for the parameters given in section 4.2.5, values for T_{OH}^{PET}, $\sum T_{I}^{\mathrm{PET}}$ and DC_{I}^{PET} were calculated and listed in table 4.2 for the MRI sequences from table 4.1. For ease of comparison, the values for T_{A}^{MRI} and DC_{A}^{MRI} were taken over from table 4.1 and located next to the corresponding PET-related parameters.

4.4 Discussion

The implementation of RESCUE with the new quick start/stop method in the Stack FPGA and the sensor parameters used results in worst-case lead times of $T_{L1}^{\mathrm{Stack}} = 980\,\mathrm{ns}$ and $T_{L2}^{\mathrm{Stack}} = 90\,\mathrm{ns} + 327.68\,\mu\mathrm{s}$. In the ideal case, the MRI triggers could be initiated at the right point in time with total lead times T_{L1} before MRI RF acquisition start and T_{L2} before RF acquisition end to reduce T_{OH1}^{PET} to zero (no PET interruption overhead time) and T_{OH2}^{PET} to a value range of no more than the PET time frame. In this case, the worst case interruption time would be

Table 4.2: Total overhead times to quick-start and -stop the DPC sensors at SDM level, total PET interruption time, and the PET interruption duty cycle for the MRI sequences of table 4.1 (© 2015 IEEE. Reprinted and adapted, with permission, from [49]).

MRI seq name	$\frac{T_R}{ms}$	$\frac{T_{OH}^{\mathrm{PET}}}{ms}$	$\sum \frac{T_A^{\mathrm{MRI}}}{ms}$	$\sum \frac{T_I^{\mathrm{PET}}}{ms}$	$\frac{DC_A^{\mathrm{MRI}}}{\%}$	$\frac{DC_I^{\mathrm{PET}}}{\%}$
T1W_aTSE	612	1.92	22.83	24.78	3.72	4.05
T2W_TSE	2400	5.11	60.96	66.07	2.54	2.75
T1W_3D_FFE	11	0.32	1.62	1.94	14.73	17.63
T2W_3D_FFE	13	0.32	4.62	4.94	35.54	37.99
EPI_7	43	2.23	26.60	28.83	61.86	67.06
Brain-T1W-FFE	25	0.32	3.27	3.59	13.06	14.36

$T_{OH}^{\mathrm{PET}} = T_{OH2}^{\mathrm{PET}} = 327.68\,\mu$s. Technically, however, due to the complexities of the two imaging modalities, this is not completely possible and the worst case value of T_{OH}^{PET} would be higher than one PET time frame.

T_{L1}^{Stack} being part of T_{L1} also depends on sensor parameters such as the validation, integration and recharge times. If the trigger from the MRI would be initiated at fixed points in time before the MRI system between RF excitation and acquisition, then T_{OH1}^{PET} would change with changing sensor parameters. If MRI trigger initiation would be adjusted or the delay between initiation and actual RESCUE procedure execution adapted according to sensor parameters, then T_{OH1}^{PET} could be kept constant. T_{OH2}^{PET} does not depend in delays related to sensor parameters. When using RESCUE with the chosen sensor parameters, the large worst-case value of T_{L2}^{Stack} (compared to T_{L1}^{Stack}) is related to the approach used to realign the DPC sensor coarse counter values with the ones of the FPGA counters during the interruption release procedure. During the interruption, the sensor dies' counters are reset to zero and all sensors' clocks launched at the beginning of a new FPGA time frame to be synchronous to the FPGAs' counters. An alternative possibility would be to store the DPC sensor coarse counter val-

ues at the moment of the clock interruption and to launch the sensor die clocks individually after reception of the release trigger when their coarse counter values match the one of the FPGA coarse counter. Some DPC sensors would start right after the trigger reception whereas other DPC sensors would be clocked after a period close to the one of the time frame in the worst case. Although this seems more attractive at first glance, two potential disadvantages may result: Firstly, in contrast to the global quick-start method, increased FPGA logic resources are needed to store and compare the sensor die coarse counter values to the FPGA's one. Secondly, for the duration of the first time frame after interruption release, not all sensor dies might acquire data in case of an individual quick-start approach. The resulting incomplete photon detection of scintillation events due to missing SiPM pixel information (4 SiPM pixels at once per die) may be discarded due to unmet Singles clustering criteria. This may be a negligible in case of one-to-one coupling (one crystal per SiPM pixel) as used in clinical PET, but is a downside for preclinical systems such as the Hyperion II^D insert where CoG algorithms are applied to cluster sensor die information from up to nine pixels to form Singles [35].
To avoid missing SiPM information during the first time frame after quick-start occurring with the method above, all sensors can be started simultaneously after MRI trigger reception regardless of their coarse counter values. As these were stored in FPGA logic when their clocks were interrupted, an offset calculation between the FPGA coarse counter at the moment of DPC sensor interruption release and each individual DPC coarse counter value can be performed to correct the scintillation events' time stamp information. This would allow for successful PET Singles clustering during the first time frame after interruption release which increases the PET sensitivity, but requires additional FPGA resources to perform offset calculations between 16-bit vectors.

In case of the conventional DPC sensor start/stop procedures, the total PET interruption overhead time is 24.2 ms when the DPC sensors are clocked at their highest JTAG frequency of 50 MHz. When solely comparing with the new quick start/stop method and its total PET overhead time lowered to the length of the PET time frame of 327.68 μs in the worst-case, the overhead-time-related PET sensitivity loss is reduced by a factor of at least 74. The above given overhead

times were determined at SDM level. When applying RESCUE at PET insert system level, the total PET interruption time would not change, as the communication between RTU, CSU and SDMs is of type digital, clocked logic. It therefore behaves deterministically in time and time-synchronously between all SDMs due to the CSU providing the same trigger and clock signals to all SDMs. The only difference at system level compared to SDM level would be a change in the RESCUE trigger lead time: Regardless of the MRI trigger source (trigger originating either from MRI system or RF coil), additional latency occurring between the trigger signal source and the SDMs via RTU/CSU due to propagation delays on cabling and digital logic would need to be taken in into account. This latency, however, is expected to be in a sub-microsecond-range because of short cabling and little amount of FPGA processing time in terms of clock cycle numbers (cycle period: 10 ns) needed to process and forward the trigger signals to the SDMs.

MRI-system-based triggering requires MR sequences to be modified by adding MR output trigger commands. This is a disadvantage compared to MRI-triggering using the RF coil electronics. The possibility to adjust the trigger lead times via sequence programming to minimise T_{OH} might seem to be of an advantage at first sight compared to hardware modifications of the RF coil electronics. However, the latter would need to be done only once where the sequence programming would need to be done for every sequence to be used which is why RF-coil-electronics-based triggering is advantageous, if trigger lead time adjustments are possible. This does not take into account the sensor-die-parameters-dependant T_{L1} variations. The addition of latency to increase T_{L1} for the sake of DPC sensor parameter flexibility could be done in the FPGA firmware of the PET system rather than via MRI sequences or in RF coil electronics hardware. Generally, the lead times T_{L1} and T_{L2} for MRI-triggering need to be determined carefully to keep the PET interruption overhead time as low as possible. On the one hand, the trigger should not be initiated too late for interruption and too late for interruption release to avoid an active PET data acquisition while the MRI in both cases acquires RF. On the other hand, if the interruption procedure is initiated very early or the release procedure started very late, larger PET overhead interruption times occur, leading to an unwanted increase of PET sensitivity loss.

The MRI measurements results (see figs. 4.10 and 4.11) demonstrated that the

noise floor increase resulting from the irradiated RF fields by the SDM during PET data acquisition is reduced when the DPC sensor clocking is interrupted. The noise level was decreased to the one of the reference scan with the SDM powered-off, meaning that RESCUE can be applied in combination with DPC sensors in a SDM to not only reduce SNR degradation, but successfully preserve the intrinsic SNR during PET/MR imaging. The aim to interrupt the PET data acquisition during every MRI RF acquisition phase for SNR preservation purposes is attended by less acquired PET coincident events available for image reconstruction when compared to a continuous PET scan during the same amount of time. Then amount of additional time needed for a PET scan during PET/MR imaging with applied RESCUE to obtain the equal number of prompt coincidences depends on the PET/MR imaging protocol (e.g. types of MR sequences used, size of subject of interest to be scanned, PET-tracer- and MR-contrast-agent-specific time constraints) and the half-life of the PET radio-isotope used. As an example, a PET/MRI scan using RESCUE with a PET interruption cycle time of 50 % would theoretically require to extend the PET scan time by more than double the time during which RESCUE was used to acquire the equivalent amount of prompts. The reason lies in the isotope's decay progressing with time, providing less prompts per time to be acquired by PET.

Table 4.2 gives an overview of values for T_{OH}^{PET} for MR sequences presented in table 4.1. T_{OH}^{PET} scales linearly with the MRI turbo factor, as the latter equals the amount of MR RF acquisition phases per MRI repetition time. As an example for a sequence with a high TF in table 4.1, the T2W_SE sequence with $TF = 16$ leads to a worst-case T_{OH}^{PET} of 5.11 ms, which causes the total PET interruption time to increase by up to 7.7% (66.07 ms) when compared to the total MRI RF acquisition time. T_R is comparatively high, though, which reduces the impact of TF combined with the low value of T_{OH}^{PET} on the total PET data interruption duty cycle ($DC_I^{\mathrm{PET}} = 2.75\%$ compared to $DC_A^{\mathrm{MRI}} = 2.54\%$). On the other hand, the impact of T_{OH}^{PET} on T_I^{PET} augments with growing fraction of the MRI acquisition time window compared to the repetition time, as noticeable for the T1W_3D_FFE and T2W_3D_FFE sequences. Sequences typically used for fast or high-resolution imaging [80] are EPI and FFE sequences as listed in table 4.2. They are often characterised by high acquisition duty cycles as in the case of the T2W_3D_FFE sequence. The latter would introduce a PET sensitivity

loss of 38 % during a PET/MRI scan using RESCUE, leading to a considerable extension of PET scan time to obtain the same amounts of coincident PET events compared to an uninterrupted PET scan. In contrast, the T1-weighted FFE and the two TSE sequences allow for a long PET data acquisition time per repetition time window ($(DC_I^{\mathrm{PET}} < 18\%)$ which makes the application of RESCUE more attractive to preserve the MRI SNR. The PET sensitivity loss related to T_{OH}^{PET} in the worst case is below 3 % for both the presented Brain_T1_FFE and the T1W_3D_FFE sequences, which is acceptable compared to the losses occurring during MRI RF acquisition which are for both sequences below 15 %.

4.5 Conclusion

In this chapter, a PET data acquisition gating technique aiming at PET-related RF interference reduction during PET/MR imaging, was presented. By MRI-synchronously interrupting the PET data acquisition during MR RF signal acquisition phases, PET-electronics-related RF emission is modified with the purpose to coupling less noise into the MRI RF coil. This, in turn, reduces the MRI SNR deterioration which preserves MR image quality. Timing-specific requirements for a PET system to perform data acquisition interruptions with time windows close to those of MR RF receive phases to avoid unnecessary PET sensitivity loss were defined. The principles of RESCUE were demonstrated using the Hyperion II^{D} platform by gating the data acquisition of the DPC sensors via clock signal interruption. As the vendor-specific procedures to safely interrupt the DPC sensor clocking do not allow for short interruption periods being in the range of MRI RF signal acquisition duty cycles, an alternative method enabling a quick-stop and -start of the DPC sensors was developed and presented. MRI SNR and noise measurements performed with a single SDM revealed that the noise floor occurring during active PET data acquisition dropped to the level of the reference noise scan (SDM powered off) when RESCUE was activated to interrupt the PET data acquisition.The presented worst-case time window calculations for the sensor clock interruption and release procedures are the same for a single SDM as well as a full PET ring, as the SDMs are all synchronised with a same reference clock provided by the central synchronisation unit. The use of RESCUE during PET/MR imaging aims at the MR image quality preservation

particularly for highly-SNR-sensitive MRI protocols, which, however, occurs at the expense of a PET sensitivity loss introduced by PET data acquisition interruptions. The higher the MRI RF acquisition duty cycle of a sequence, the worse the PET sensitivity loss. The evaluation, whether to use RESCUE or not would therefore depend on the particular PET/MR image protocol used. This implies amongst others the types, parameters and duration of MR sequences, the PET scan type (static or dynamic), PET tracer type and half-life of the PET isotope, the PET/MRI ROI size and the physical conditions of the subject to be imaged.

Chapter 5

FPGA-based RF interference reduction for simultaneous PET/MRI using digital clock frequency shifting

5.1 Introduction

The MR-synchronous gating method presented in chapter 4 to reduce the PET-related RF interference during simultaneous PET/MR imaging has the disadvantage that the PET sensitivity decreases with an increasing MRI RF acquisition duty cycle. This leads to less PET coincident events for PET image reconstruction resulting in PET images with lower SNR compared to an uninterrupted PET scan during the same scan time. An increase in PET scan time to acquire an equal number of coincidences compared to a scan without PET data acquisition interruption would be necessary. Depending on boundary conditions of a proposed PET/MR imaging protocol (see end of section 4.5), an increased PET scan time or a sensitivity loss for a same scan time might yield unsatisfactory results for PET and thus not be acceptable as a trade-off to preserve the MRI SNR. To overcome this disadvantage while still being able to reduce RF field coupling into the MRI RF receive chain, a different method with initial investigations is presented in this chapter. This method aims to modify the RF fields emitted

by the PET electronics residing within or in close proximity to the MRI bore and, like RESCUE, focuses on the digitally clocked electronics being particularly prone to RF field generation as described in section 2.4.3.
The RF emission are modified by shifting frequencies of the clock signals so that the resulting emission amplitudes in the MRI-sensitive frequency range are reduced and thus lower the noise coupled into the MRI RF coil(s). The proof of concept was implemented and studied using the Hyperion II^D MR-compatible PET platform and the clock frequency shifts were implemented solely by adaptations to the FPGA firmware. Reconfiguring FPGA firmware in the field with regard to adaptive RF interference reduction may allow expansion of application-related possibilities of PET/MRI systems. Whereas RESCUE aims at expanding the range of SNR-critical MRI protocols possible during simultaneous PET/MRI, for the proposed method, the RF emission spectra of a PET subsystem could be adjusted depending on the type of MRI RF coil used. In addition to a body coil, this would allow the use of dedicated smaller MRI coils (e.g. for head- and breast-imaging) with the same PET/MRI system with PET detectors close to the coil and optimised PET RF emission to aim for the highest MRI SNR preservation. Likewise, adaptive RF interference reduction methods may allow the combination of the same PET detector with different MRI systems using different B_0 field strengths by adjusting RF emissions with respect to the different Larmor frequencies.
The remaining sections of this chapter introduce the two-step measurement approach that was applied to investigate the clock-frequency-shift-based interference reduction method:

1. Broadband RF measurements performed with lab bench measurement equipment using a single singles detection module (SDM) to analyse the RF emission spectra resulting from clock frequency adjustments.

2. MRI noise measurements to evaluate the reduced PET-related RF interference.

This is followed by the presentation of the measurements results. Finally, the latter are discussed to evaluate the proof-of-concept of the RF interference reduction method.

5.2 Methods

5.2.1 Clock frequency shift method: Introduction and experiments

All coils designed to receive signals from EM fields are characterised by resonance modes.These are areas within the frequency spectrum where energy of RF fields with frequencies matching those of the modes is transmitted to the coil with a high efficiency. As an example, the resonance spectrum of the Hyperion II^D mouse birdcage coil is shown in fig. 5.1. It was determined by measuring the reflection coefficient (S11) over a frequency range between 50 and 150 MHz. The mode used for MRI RF signal reception is highlighted in fig. 5.1 by the grey-shaded area. The coil is tuned to be resonant at the Larmor frequency of 127.78MHz at 3 T. All other coil modes at lower frequencies are not used for MRI acquisition. The signal provided by these is therefore suppressed by the MRI receive chain by applying a band-pass filter with a centre frequency being the Larmor frequency.

By adapting PET-detector-related clock signal frequencies in such a way that

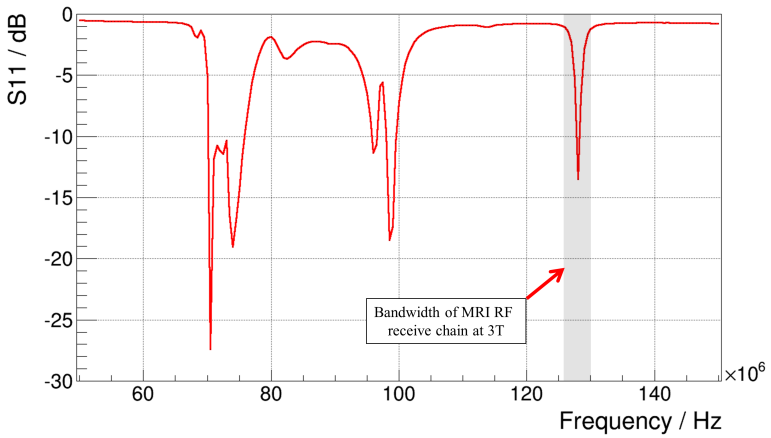


Figure 5.1: Resonance spectrum of the mouse birdcage coil measured with a network analyser (Agilent E5071C ENA). It visualises the resonator modes at which the energy transmission of the coil is highly efficient. The grey-shaded area represents the MRI-sensitive frequency bandwidth at the Larmor frequency for a 3-T MRI (Figure reprinted from [148]).

the resulting amplitudes of the RF fields emitted by the PET detector are reduced within the range of the Larmor frequency, the PET-related noise coupling

into the RF receive chain of the MRI is expected to be lowered.
The impact of clock signal frequency shifts on resulting RF fields were studied using a single SDM equipped with six detector stacks, and which was directly connected to a control PC. The capabilities of the clock infrastructure provided by the DACA (presented in chapter 3) offer the possibility to shift the typical sensor die clock frequency of 200 MHz to other frequencies. The following frequencies were chosen for the investigations in addition to 200 MHz which was defined as the reference frequency:

- 100 MHz: This was chosen because of its second harmonic being the typical DPC sensor clock frequency of 200 MHz.
- 127.78 MHz: Clocking the sensor dies with the Larmor frequency of the 3-T MRI will demonstrate the maximum impact of the sensor die frequency shift on the RF fields generated and coupled into the RF coil, as the noise coupling is expected to be strongest at this sensor die clock frequency.
- 140 MHz: This frequency is in proximity of the Larmor frequency. Therefore, the noise coupling is expected to be lower than the one resulting from a die clock frequency equal to the Larmor frequency.
- 160 MHz: This one lies between the typical sensor die clock frequency and the frequencies being with or very close to the 3-T-MRI-sensitive frequency bandwidth.

5.2.2 SDM operation with different sensor die clock frequencies

For single-SDM operation, the SPU FPGA is configured to source the refCLK signal via the oscillator on the SPU, as the CSU is not available (see clock infrastructure diagram in fig. 3.10). All clock frequencies used within the SPU-FPGA, for digital components on the SPU, and for communication between the FPGAs are kept identical to those used during typical operation of the insert. For this study, only the sensor die clock frequencies are modified to the desired frequency settings by reconfiguring the stack FPGA firmware, so that the settings of the

FPGA-internal clock generator, which clocks the DPC sensors and the FPGA-internal DAQ chain, are adapted accordingly. This means that only parts of the stack-FPGA-internal logic and single-ended traces between the interface board and the sensor tile are affected in terms of frequency modification. Reconfiguration of the stack FPGA clock generator is performed by reconfiguring the complete FPGA using the SPU FPGA's internal FPGA configuration module and the Hyperion software. This allows for frequency modifications without the need to physically access and potentially displace the SDM for the sake of measurement results comparability.
To verify the correct PET DAQ functionality of the SDM when clocked at different frequencies, singles measurements were performed using a ^{22}Na source with 3.95 MBq of activity. The sensor die settings were set to values typically chosen for PET scans with the complete insert (found in [160]) and a Centre-of-Gravity (CoG) algorithm was used for PET singles clustering of the acquired raw data sets [35]. For all characterisation measurements described in the next section, the SDM was operated as follows: After power-off, the stack FPGAs were configured with firmware yielding the desired sensor die clock frequency and the SDM was configured for stand-alone operation. Then, the PET DAQ was started to enable the sensor die clocking which served as the starting point for RF-field-related measurements.

5.2.3 Characterisation

5.2.3.1 Broadband emission scans

The RF field spectra emitted by the SDM were characterised in detail by using a round-shielded magnetic-field probe ((Langer EMV, RF-R 400-1, Bannewitz, Germany) with a diameter of 25mm which was connected to a spectrum analyser (Agilent N9320B, USA). This measurement setup allows the acquisition of emission spectra over a broader frequency range than can be acquired by the MRI. It gives a better overview on the amplitude distribution for a frequency range covering the clock frequencies used in the SDM's digital electronics. Additionally, changes in the RF field distribution related to changes of the sensor die clock frequency can be studied. On a bench setup as shown in fig. 5.2, the field probe was attached to a XYZ-table equipped with a positioning system (OWIS GmbH,

Germany) and the probe was placed on the top centre of the SDM and as close as possible to the carbon fibre housing. For all of the five different clock frequencies, spectra were acquired between 50 and 250 MHz.

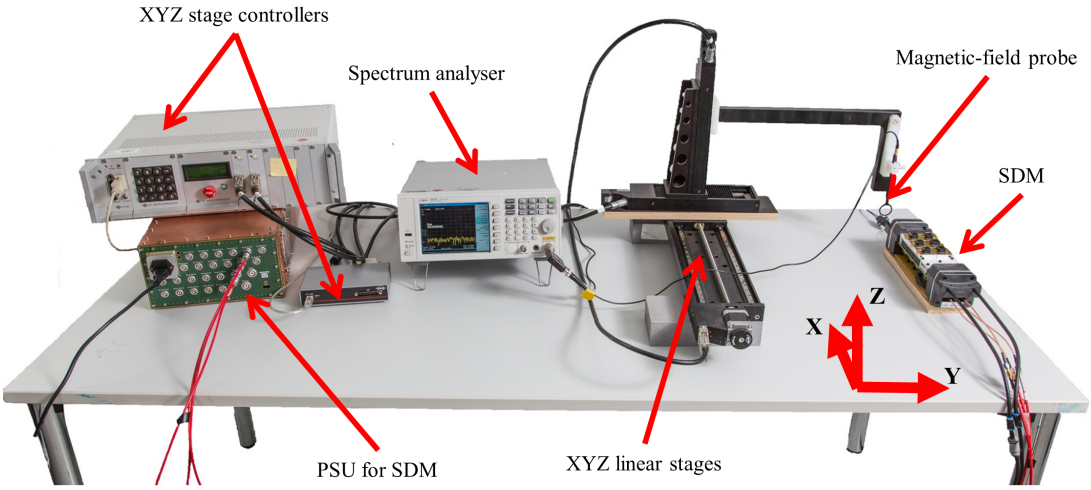


Figure 5.2: Overview of the lab bench setup used for RF broadband measurements and RF field maps (the latter is the subject of chapter 6). Not shown on the picture are the cooling unit and the control PC with the Hyperion Software which is directly connected to the SDM on the lab bench (Figure reprinted from [148]).

5.2.3.2 MRI noise measurements

To evaluate the PET-related RF interference resulting from the SDM operated with different DPC sensor clock frequencies, MRI noise scans were performed using a 3-T MRI (Philips Achieva 3.0T, The Netherlands) and modified TSE sequences as described in section 4.2.5. The RF shielding was removed from the SDM to allow unattenuated RF field coupling from the PET module into the MRI RF receive chain. This allows for larger differences in the measured noise amplitude between the measurements with different clock frequencies. The SDM was mounted on a separate gantry at the most sensitive location in terms of RF coil noise coupling as shown in fig. 5.3. The determination of that location was done by performing noise scans for each of the 10 SDM gantry positions using the stack FPGA reference firmware design (sensor die clock frequency: 200 MHz).

Additionally, the influence of frequency shifts on the noise generation related to signal switching along the downstream data paths excluding the sensor tiles

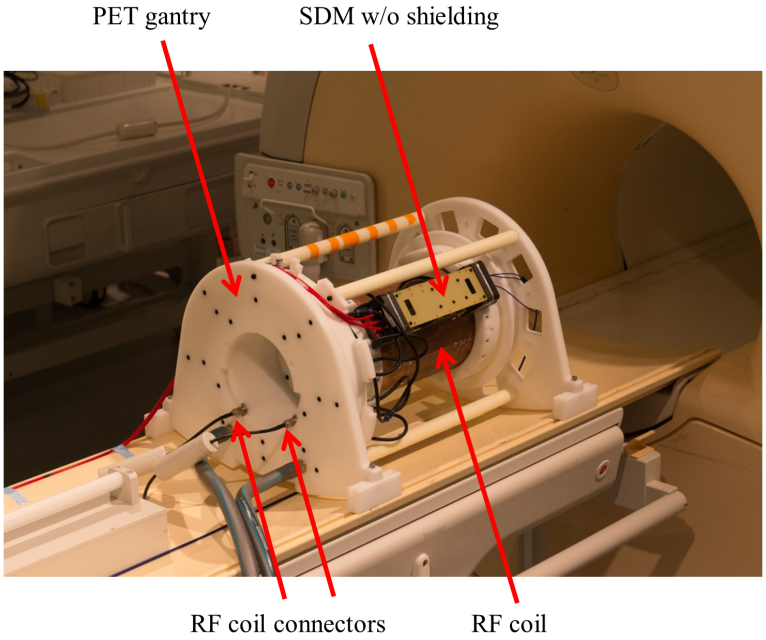


Figure 5.3: One SDM with removed RF shielding was mounted on a spare gantry to study the influence of the sensor die clock frequency on the noise coupled into the MRI RF receive chain (Figure reprinted from [148]).

was examined to demonstrate that RF-field-emission-related RF interferences are not restricted to the sensors and "single-ended" signal traces. The stack-FPGA-internal dummy data generators were used to vary the data transmission rate and thus the signal switching over time within the stack FPGAs, SPU-FPGA and the LVDS data lines between the FPGAs. In order to analyse how the noise coupling is modified by changes regarding the switching-behaviour, two MRI noise measurements with different message data rates generated by the dummy data generators (DDG) (see section 3.2.3.2 paragraph *Stack FPGA design*) were performed. One noise scan was done with the FPGA-internal message data generation set to the lowest setting (one data message per sensor die and frame count being equal to 16 incoming DPC sensor data messages from the sensor tile per time frame count) and a second one was done with a high dummy data message rate setting of 25 data messages per sensor die and frame count (equals 400 DPC sensor messages per frame count). While the DDGs were active, the sensor die clocking remained deactivated to be able to measure noise generation solely related to the downstream data path operated at different DDG message rate settings. For

comparison purposes, a third noise measurement was performed with the SDM clocking the DPC sensors while the stack FPGAs' processing chain clock was disabled so that no FPGA-internal and LVDS-communication-line-signal switching related to sensor data acquisition took place. For these measurements, the stack FGPA firmware design was used which clocks the sensor dies at 200 MHz. The noise measurement results are compared with a reference scan during which the SDM was off-powered.

5.2.3.3 MRI SNR measurements

The influence on MR imaging caused by SDM data acquisitions at different sensor die clock frequencies was evaluated by imaging a cylindrical phantom filled with 20 ml of a $CuSO_4$ solution placed inside the Tx/Rx mouse coil. To visualise SNR differences caused by a single SDM operated when operated at different frequencies, a 2D Turbo-Spin-Echo (TSE) sequence (T_R/T_E = 400/157.46 ms, Flip angle: 90°, turbo factor (echo train length): 12, Voxel size = $0.07 \times 0.07 \times 0.5\,mm^3$, number of slices: 1, FoV-size: $80 \times 80\,mm^2$ acq. matrix: 1144×1144, recon. matrix: 1600×1600) was used which aimed at very high resolution MR images at low SNR. The SDM position on the PET gantry was same as the one chosen for the MRI noise scans (section 5.2.3.2). The signal intensities were determined along a line profile horizontally with a line width of 50 pixels in the MR image crossing the phantom at its centre. As the intensity values in the region within the phantom were comparable for the three images, the intensity values of the line profiles were normalised to the mean intensity of the values within the phantom for each image and the values averaged over 10 histogram bins. Then, the mean noise level was calculated for each line profile, thereby allowing the determination of noise floor changes related to the SDM acquiring sensor data at different DPC sensor clock frequencies.

5.3 Results

5.3.1 SDM operation

By measuring the different sensor die clock frequencies generated by the different stack FPGA designs with an oscilloscope (Tektronix MSO4014, USA), the

clock-related implementations were successfully verified. The mean singles rates obtained with PET singles measurements and the stack firmware designs generating sensor die clock frequencies as listed in section 5.2.1 are depicted in fig. 5.4 with variations between 115.4 and 118.3 kcps.

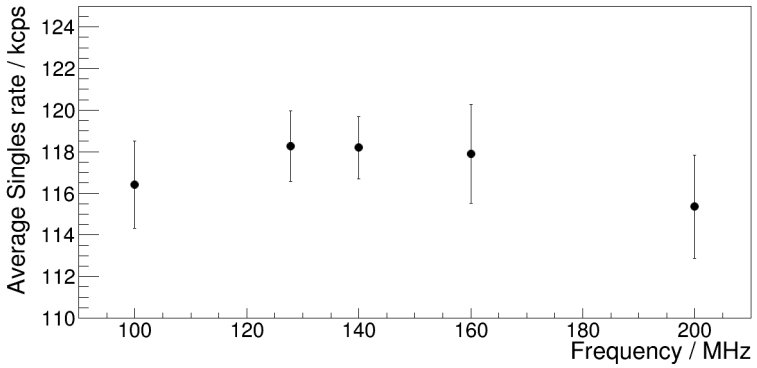


Figure 5.4: Mean singles rates obtained with firmware designs yielding different sensor die clock frequencies of $100, 127.78, 140, 160$ and $200\,MHz$. The error bars indicate standard deviations (Figure reprinted from [148]).

5.3.2 Characterisation

5.3.2.1 Broadband emission scans

The broadband emission measurement results obtained with the field probe and the spectrum analyser are summarised in fig. 5.5(a). The RF emission spectra generated by the SDM differ considerably depending on the frequency of the generated sensor die clock signal. Within the MRI-sensitive frequency range, the spectra with lowest amplitudes are generated by the firmware designs with clock frequencies of 160 MHz (red) and 100 MHz (light blue). The intentional worst-case scenario, where dies are clocked with 127.78 MHz, leads to highest emission amplitude within the grey-shaded area. It is followed by an FPGA design clocking the sensor dies at 140 MHz (green). Figure 5.5(b) visualises the emission spectra within the frequency bandwidth which is also covered by the MRI noise scans (1 MHz range with 127.78 MHz as the centre frequency). Here, the spectrum obtained with a die clock frequency equalling the Larmor frequency was not included for better distinction between the spectra obtained with all other clock frequencies. Again, amplitudes resulting from the 160 MHz design are

lowest, whereas those of the 140 MHz design are highest (when not considering the worst-case scenario).

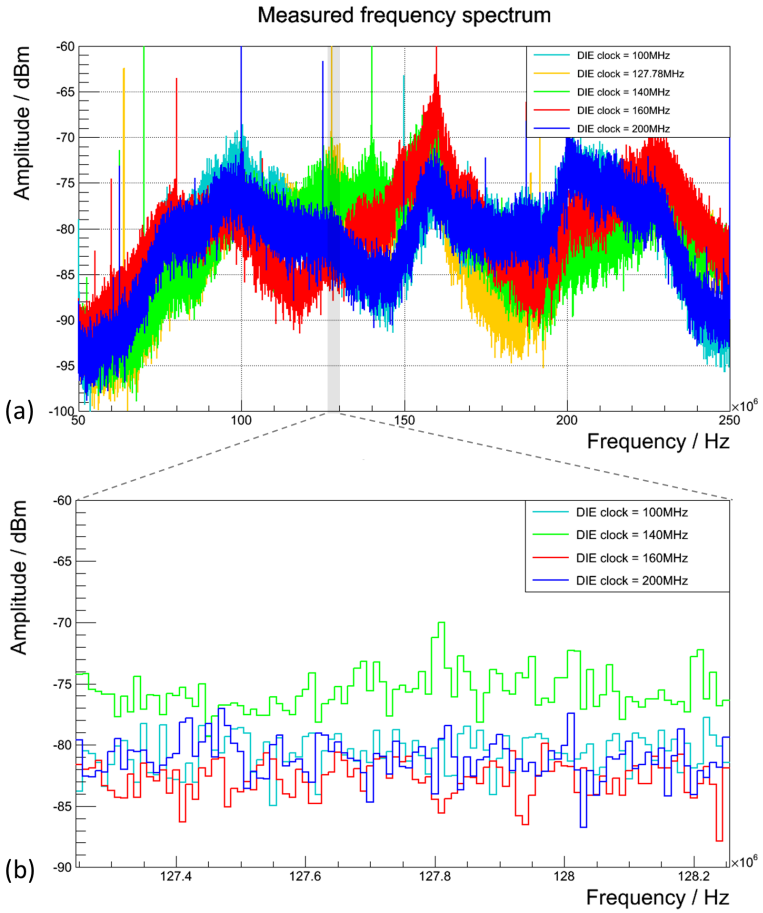


Figure 5.5: Lab bench measurements of the emission spectra obtained with one SDM: Diagram (a) depicts the spectra amplitudes over a frequency range between 50 and 250 MHz. In diagram (b) are shown the amplitudes within a bandwidth of 1 MHz in the region of the grey-shaded area in diagram (a) corresponding to the bandwidth of the 3-T MRI (Figure reprinted from [148]).

5.3.2.2 MRI noise measurements

For the worst-case scenario where an SDM performs a PET data acquisition with a die clock frequency equal to the Larmor Frequency of the 3-T MRI while the MRI acquires RF signal via a noise scan, the measured floating point (FP) values are four orders of magnitude higher than noise amplitudes measured while clocking the dies with other frequencies. The noise measurement results for the

latter excluding the worst-case scenario are shown in fig. 5.6. The reference noise scan was acquired while the SDM was powered off. The clock frequency of 140 MHz led to highest noise amplitudes with FP values over 350. FPGA designs generating frequencies of 100 MHz and 160 MHz resulted in lowest noise levels compared to other frequencies.

Figure 5.7 illustrates the noise scan results obtained for the case of dummy data message transmissions using the stack-FPGA-internal DDGs while the sensor die clocks remain disabled and the case where only the sensor dies are clocked while the processing chain clock of the stack FPGAs are disabled. When operating the DDGs with the sensor dies being inactive, the noise floor level does not increase for the two different message data rates compared to the reference scan, but distinct noise peaks with high amplitude appear for the high message rate scenario. Clocking the sensor dies so that they acquire data while the remaining downstream data path remains inactive due to the disabled stack-FPGA-internal processing chain clocks raises the entire noise floor in addition to distinct noise amplitude peaks.

5.3.2.3 MRI SNR measurements

Figure fig. 5.8 shows three MR low-SNR images of a phantom shown in fig. 5.8. Image fig. 5.8(a) was acquired while the SDM was off-powered, fig. 5.8(b) was done while the SDM was acquiring data with the DPC sensors clocked at 160 MHz, and fig. 5.8(c) was taken during a PET DAQ with a sensor die clock frequency of 140 MHz. The image quality of (b) degrades during PET DAQ at 160 MHz compared to the reference scan (a) and further degrades when operating the SDM at 140 MHz as seen in (c).

The RF signal intensity line profiles determined for the three measurements and normalised are depicted in fig. 5.9. The reference scan leads to the lowest noise floor of the three images with a noise mean value of 0.722 ± 0.004 (SNR: 1.385). When the SDM is operated, the sensor die clock frequency of 160 MHz leads to the lowest noise (mean value: 0.800 ± 0.004, SNR: 1.25), a frequency of 140 MHz results in the highest one with a mean value of 0.839 ± 0.004 (SNR: 1.192). With respect to the noise floor measured during the SDM operation with 160 MHz, the relative difference to the noise floor at 140 MHz equals 4.88 %.

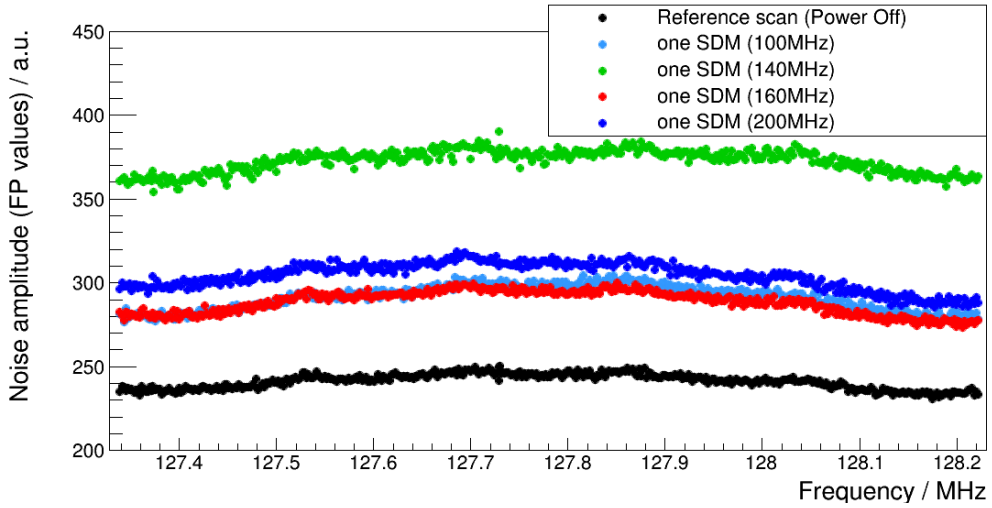


Figure 5.6: Noise measurement results obtained for the different sensor die clock frequencies except 127.78 MHz. The reference scan was performed with the SDM switched off (Figure reprinted from [148]).

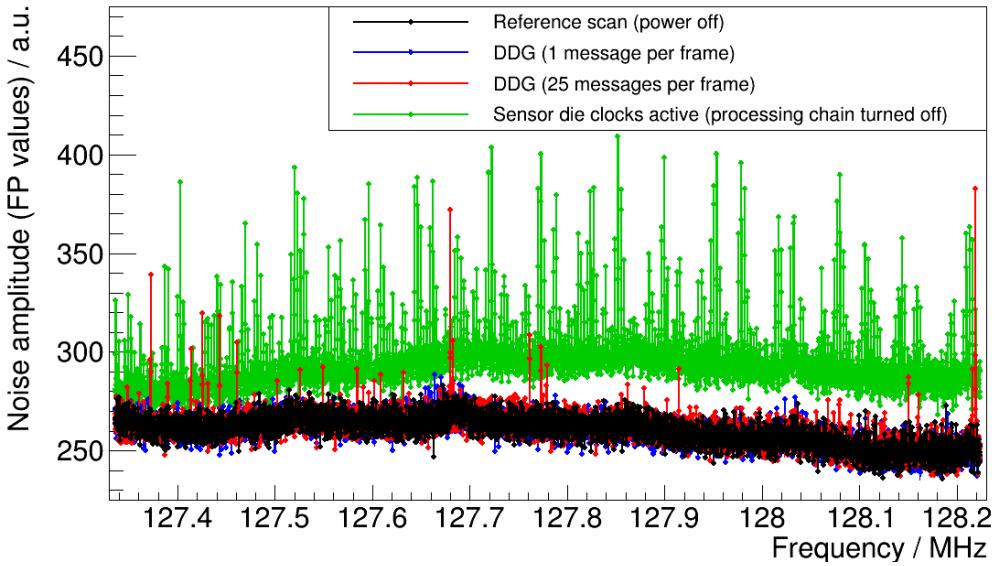
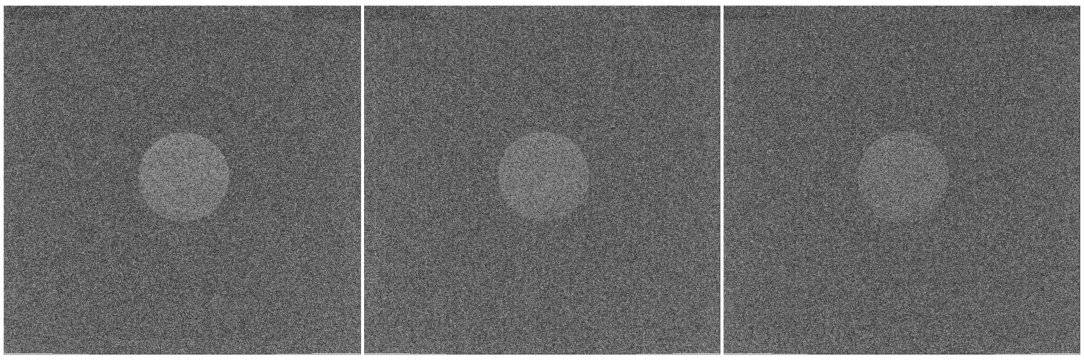


Figure 5.7: MRI noise measurements performed using stack-FPGA-internal dummy data generators with two different message rates and no sensor die clocking compared to the case where only sensor die clocks are active while the DACA-wide processing chain is deactivated.



(a) SDM powered off **(b) Clock frequency = 160MHz** **(c) Clock frequency = 140MHz**

Figure 5.8: MR phantom imaging performed with low SNR while (a) the SDM is is off-powered, (b) the SDM acquired PET DAQ at 160 MHz, (c) the SDM was operated with a DPC sensor frequency of 140 MHz (Figure reprinted from [148]).

5.4 Discussion

5.4.1 SDM operation

The singles rate measurement results shown in fig. 5.4 demonstrate that the PET DAQ is successfully performed by the SDM when using firmware designs to clock the sensor dies with variable clock frequencies. As some of the DPC sensor configuration parameters result in time periods of clock cycle units (T_{CK}), their values may need to be revised when changing the clock frequency as the time period values resulting from frequency changes are modified, too. This applies to the validation, integration and recharge times which would need to be adapted if detector-specific DAQ behaviour for data acquisitions is aimed to be kept while changing the frequency for RF interference reduction purposes. This constraint was taken into consideration for the measurements described in section 5.2 and the parameters were adapted depending on the clock frequencies as listed in table 5.1.

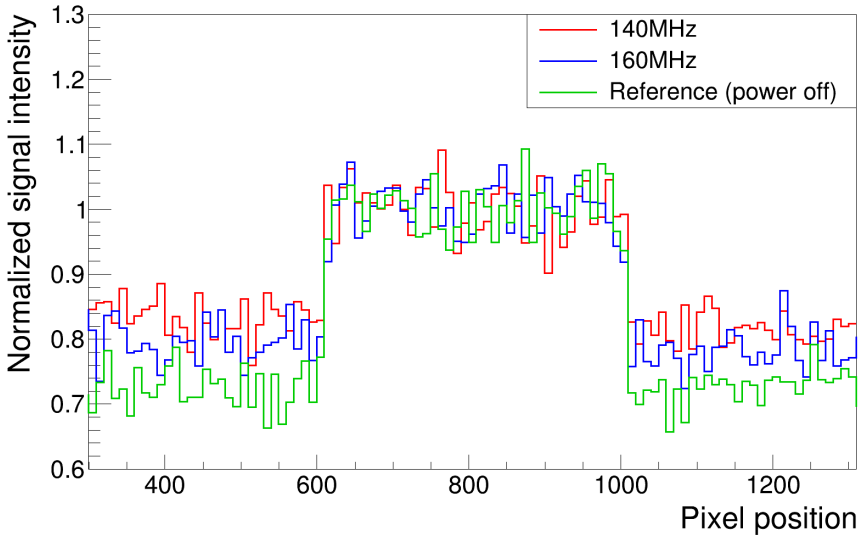


Figure 5.9: Signal intensities across a horizontal line profile crossing the MRI phantom: The noise floor varies depending on the sensor die clock frequency generated by the SDM firmware (Figure reprinted from [148]).

Table 5.1: Clock-frequency-dependent DPC sensor parameters for 200 MHz adapted to values for different frequencies to result in similar absolute time periods.

Clock [MHz]	Validation [t_{CK}]	Validation [ns]	Integration [t_{CK}]	Integration [ns]	Recharge [t_{CK}]	Recharge [ns]
200	**8**	**40**	**33**	**165**	**2**	**10**
160	8	50	33	206	2	13
140	4	28	17	121	1	7
127.78	4	31	17	133	1	8
100	4	40	17	170	1	10

The parameter set typically chosen for a clock frequency of 200 MHz served as the reference [160] and is bold in table 5.1. When choosing 100 MHz as a die clock frequency, most of the settings can be set to half the amount of clock cycles to obtain the same time periods compared to those for 200 MHz. However, time periods resulting from frequencies between 100 and 200 MHz increase in difference from the reference time periods, the more a frequency equalling 150 MHz is approached. This very likely explains why the mean Singles rates in fig. 5.4 slightly differs towards the frequency of 150 MHz and decreases again when ap-

proaching a clock frequency of 100 MHz.
Furthermore, a reduction of the DPC sensor clock frequency has an impact on the dead-time properties of the sensor. Affected are the minimum amount of time needed to successfully detect two consecutive scintillation events as well as the bandwidth limitation regarding the message data rate. These frequency-dependent effects are related to the clocked logic (the FSMs) of the DPC sensor's main acquisition controller. As its behaviour is deterministic, the theoretical bandwidth limitation, which is dependent on the clock frequency, can be predicted when assuming triggering from the validation network as soon as the event-acquisition-FSM is in *ready*-state (fig. 4.2). Taking into account this constraint, simulations with scintillation event distributions provided e.g. by GATE [171] can be performed to determine clock-frequency-dependent count rate limitations which is of particular importance for PET scans dealing with high count rates.

5.4.2 Characterisation

The EM field coupling efficiency between an RF coil and EM field sources strongly depends on EM field amplitudes at frequencies in the range of the resonator modes (fig. 5.1). Consequently, components of the spectrum with high amplitudes should be eliminated in or shifted away from theses frequency ranges to reduce unwanted, spurious signal being coupled into the RF coil. This principle was successfully demonstrated by spectra measurements of EM fields from an SDM by modifying the frequency of clocked, digital circuits (fig. 5.5). In the case of the SDM serving as the platform for the proof-of-principle, the clock frequency of the sensor die clock was chosen to be altered, as this clock signal is transmitted via signal traces between interface boards and sensor tiles of all stacks using the "single-ended" transmission standard. The latter is more prone to EM field radiation compared to other standards such as LVDS and therefore more likely to generate field-related disturbances (see section 2.4.3). Thus, one expects a larger impact on EM field spectra changes when changing the sensor die clock frequency. This is depicted by the distinct amplitude peaks in fig. 5.5 at frequencies equal to the modified sensor die clock frequency. Generally, the broadband spectra covering the entire measurement frequency range result from superposition of a lot of EM field sources which includes periodic as well as non-

periodic electrical signal changes in components, connectors and PCB traces. For instance, a different sensor die clock frequency will also result in a change of generated EM field characteristics caused by modifications in non-periodic switching of the DPC sensor data output lines. A good example is given by the spectra and noise measurement results obtained with a sensor die clock of 140 MHz: Despite being outside the MRI-sensitive bandwidth, this frequency leads to increased EM field radiation in the area of the Larmor frequency at 3T (see green plots in fig. 5.5) which considerably raises the noise floor (green plot in fig. 5.6). Therefore, the choice of clock frequencies suitable to reduce the spectra amplitudes within the MRI-sensitive bandwidth is not trivial and requires measurements with spectrum analyser equipment and MRI noise measurements using the RF coil for which the PET detector shall be optimised regarding EM field emission. The results shown in fig. 5.6 for 100 MHz and 160 MHz demonstrate that properly chosen clock frequencies may help to lower the noise coupled into the RF coil by a PET detector using digital electronics in the MRI bore. Although in case of the SDM, the sensor die clock frequency for the DPC sensor was shifted, this principle applies to digital, clocked electronic circuits in general and is not limited to the DPC sensor being a dSiPM. This is demonstrated in fig. 5.7 with the noise measurement result obtained with disabled sensor die clocks but with running stack-FPGA-internal PET data processing chain which was operated at a high dummy data message transmission rate. The distinct noise amplitudes reveal a modified EM field emission with regard to digital signal switching. The broadband noise floor, however, is not increased, compared to the reference scan and the measurement during which synthetically generated DPC sensor message data is processed and transmitted at a low rate. In contrast, the entire noise floor is raised and the noise peaks related to digital switching appear when the DPC sensors acquire data while the FPGA-internal data processing chain remains off due to disabled processing chain clocks. This measurement demonstrates that the DPC sensor operation via the single-ended traces of the interface board and the sensor tile plays a dominant role regarding noise coupling when compared to the remaining communication and clocking paths of the SDM. Investigations in this direction by performing further measurements may help to improve the PCB design in terms of signal transmission types for future PET module designs in order to further reduce RF interferences in addition to clock frequency adjust-

ments.

The intrinsically low SNR of the MR phantom image obtained with the 2D-TSE MRI sequence while the SDM was off is visualised in fig. 5.8(a). Comparing fig. 5.8(b) and fig. 5.8(c) yields visible differences in MR image deterioration depending on the frequency used for the DPC sensor clocking of the SDM. The line profile comparisons of the three images showed that the SNR degradation was a result of an increase in the noise floor which is related to SDM-related RF interferences. Differences in the noise floor level obtained during 140 and 160 MHz clocking demonstrate that clock frequency adjustments may successfully be used to lower PET-electronics-related noise coupled into the MRI RF coil.

Any counts detected by the DPC sensors during the SNR measurements originated from LYSO-related radiation as well as dark counts created by semiconductor-related thermal excitation and corresponds to the conditions chosen for the MR noise measurements and spectrum analyser measurements performed with the lab bench setup. The only exception to this were the singles measurements. Using a radioactive source to generate scintillation events modifies the signal switching behaviour in terms of patterns as well as its frequencies due to an increased PET data message transmission between the DPC sensors and the stack FPGAs and between the stack and the SPU FPGA of an SDM. This may modify the RF field emission to couple more noise into the MRI RF coil, which would further illustrate differences in MRI SNR degradation on higher orders of magnitude depending on the sensor die clock frequency. However, this could not be investigated, as the use of radioactivity was not allowed in the MRI facility where the SNR measurements took place. Investigations implying a measurement setup using a complete PET ring rather than a single SDM combined with coils located closer to the PET detector (such as a large birdcage coil [125]) are expected to reveal stronger negative impacts in MR image quality for a broader range of sequences which is to be considered as next research steps.

5.5 Conclusion

In this chapter was presented a possibility to reduce PET-related RF interferences created by PET detectors which incorporate digital electronics within or in the vicinity of the MRI bore. By adjusting frequencies of clock signals driving

digital circuits, the EM fields irradiated by the PET detector can be modified to reduce the RF field amplitudes within the MRI-sensitive RF bandwidth. This, in turn, reduces the noise coupled into the MRI RF coil and thus preserves MRI SNR.

Initial investigations were performed with one Hyperion II$^{\mathrm{D}}$ SDM by solely modifying FPGA firmware to generate clock frequencies for the DPC sensor clock different than the typical 200 MHz. Broadband spectrum analysis on a lab bench and MRI noise measurement studies using clock frequencies of 100, 127.78, 140, 160 and 200 MHz demonstrated that noise coupled into the MRI RF coil by the PET detector can be reduced when clock frequencies are well-chosen. Whereas RESCUE as an RF interference reduction technique presented in chapter 4 may be used to expand the range of SNR-critical MRI protocols for simultaneous PET/MRI, the frequency-shift approach offers the possibility to reduce RF interferences without the need for PET DAQ gating. In case of the SDM-based DPC sensor clock frequency modifications via firmware, the field emission could be adjusted in-the-field depending on the type of MRI RF coil used to optimise the PET detector with regard to the particular RF coil used. Dedicated RF coils could then be used with a same PET/MRI system with its PET detectors being close to the coil thanks to optimised PET RF emission to preserve MRI SNR. Another possibility would be the combination of a same PET detector with different MRI systems using different B_0 field strengths thanks to possible adjustments of the RF emission with regard to different Larmor frequencies.

Chapter 6

FPGA-based RF interference reduction for simultaneous PET/MRI using digital clock phase shifting

6.1 Introduction

The RF interference reduction method presented in chapter 5 aims at MRI SNR preservation by applying frequency shifts of clock signals used for digital, clocked PET electronics. The frequency shifts result in a modified spectrum of the RF field emitted by the PET detector. By adjusting these frequencies so that the spectral amplitudes of the irradiated RF fields are reduced within the frequency range, the MRI RF receive chain is sensitive to, the spurious signal coupling can be lowered in order to preserve the MRI SNR during simultaneous PET/MR imaging.

Besides the clock frequency adjustment method, another possibility to reduce the noise coupling into the MRI RF coil via EM field emission modifications may be obtained by changing the phase relationship between periodic signals that are transmitted electrically. Generally, such a change in phase relationships not only introduces modifications of the EM field spectrum amplitudes. The irradiated EM field of an electronics device is the result of a plurality of superimposed fields

that are generated by each of the electrically switching signal traces which in case of periodic switching act as antennas [137]. By changing the phase relationship of adjacent signals with the aforementioned properties so that their electrical signal values are always opposite to each other, the resulting EM fields should mitigate each other according to wave theory, thereby changing the spatial EM field distribution. When applying this hypothesis to a PET detector using digital, clocked electronics, the field distribution can be modified to obtain a coupling efficiency reduction between the external RF fields and the MRI RF receive coil in order to lower the RF interference between the PET detector and the MRI. In this regard, the coupling is defined by the coefficients of the externally emitted RF fields' mode expansion in the mode base function of the RF receive coil. The coefficients are determined by the coupling integral.EM field distributions (or pattern) that result in smaller coupling coefficients yield a reduced energy transmission efficiency because of an increased RF coil mode excitation.
This chapter presents investigations related to the clock phase shift approach. Similar to chapter 5, implementations and studies were performed using a single Hyperion II^{D} SDM by solely changing FPGA firmware to modify clock phase relationships between different clock signals. The studies presented in this chapter are divided into three different parts. The first one deals with calculations and simulations of the RF field distribution and its coupling to the RF resonator. Afterwards, RF field distributions measurements are performed with the lab bench measurement equipment presented in chapter 5 to study distribution modifications resulting from clock phase shifting. Finally, initial MRI noise measurements with a 3-T MRI were performed to demonstrate the impact on noise coupled into the RF mouse coil.

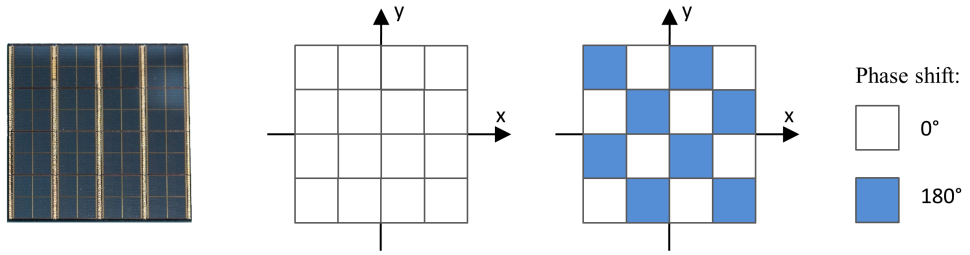
6.2 Methods

6.2.1 Simulations of the clock phase shift method

6.2.1.1 Field emission distribution

In order to analyse the feasibility of the method, a model based on the Hyperion II^{D} sensor tile as shown in fig. 6.1(a) was implemented. As the tile represents

a symmetric arrangement of 4×4 sensor dies which are clocked via "single-ended" signal traces (see section 2.4.3 regarding trace type), the sensor dies were modelled as 16 EM field sources. To keep the model simple, every emitter was modelled as a magnetic dipole which yielded a dipole emitter system spatially arranged as the real sensor tile as drawn in fig. 6.1(b). This model was then used to calculate the emitted magnetic field distributions in a plane parallel to and 35 cm away from the sensor tile surface using MATLAB. This allowed to investigate in superposition effects of the EM fields when the dipoles oscillate with phase relationships being out of phase between different dipole emitters. Two scenarios were compared: An in-phase model where the clock phase relation between all dipoles is equal to zero (fig. 6.1(b)), and a checkerboard model where the phase difference between adjacent dipoles corresponds to 180° as visualised in fig. 6.1(c). The latter pattern was chosen due to expected compensational superposition effects related to the field emission.



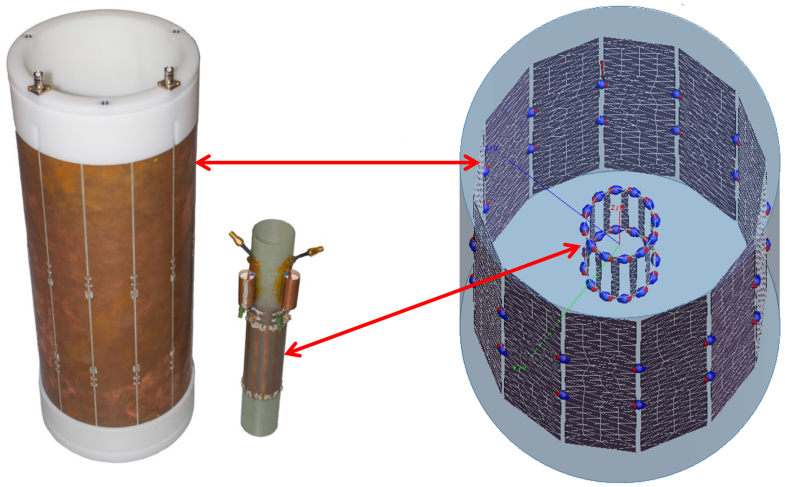
(a) Sensor tile (b) In-phase pattern (c) Checkerboard pattern

Figure 6.1: Phase shift method: Each DPC sensor of a sensor tile (image (a)) was modelled as a dipole loop. Image (b) shows the in-phase pattern model, image (c) illustrates a checkerboard-phase pattern (Figure reprinted from [148]).

6.2.1.2 Field coupling simulation

As a next step, noise coupling simulations using a finite element method (FEM) tool-kit from FEKO [172] were performed to study the noise induction created by external sources and coupled into a birdcage resonator. The simulation included an implemented FEM model of the birdcage mouse coil with its RF screen as shown in fig. 6.2 and the dipole arrangement (as introduced in section 6.2.1.1) placed in front of the RF screen which surrounds the RF resonator. Based on this model, current distributions induced in the RF coil by the magnetic field

component of the external field to be irradiated by the dipoles were simulated for both cases of in-phase and the checkerboard-phase pattern oscillation. The dipoles' frequency was set to the resonant frequency of the RF coil, so that the energy coupling could be studied at an operating point at which field energy is transferred to the coil with highest efficiency. This allowed the differences in simulated noise coupling related to variable field pattern to be maximised.



(a) MRI RF coil screen (left), RF coil (right) (b) FEKO simulation model

Figure 6.2: Image (a): The RF screen and the RF mouse coil placed next to it. Image (b) depicts the FEM simulation model [172] of the coil and the screen (Figure reprinted from [148]).

6.2.2 SDM operation using sensor die clock phase shifts

The EM field emission changes studied with the MATLAB model (section 6.2.1.1 were based on a dipole model representing the DPC sensor clock phase relationships at stack level. Modelling only the sensors and their clock traces does, however, neglect all other electronic components, connectors and signal traces of one entire detector stack. The same applies to the SPU board, as it also contributes to the field emission of a complete SDM. Thus, measurement-related investigations of RF interference changes introduced by clock phase pattern modifications were performed not with a single sensor tile, but with a fully equipped SDM. To map the checkerboard phase pattern introduced at stack level to SDM

level, the clock phase variations were applied between complete stacks and phase differences between adjacent sensor tiles was set to 180° to remain consistent with the phase shifts used for the calculations and simulations. A diagram of the checkerboard phase pattern arrangement at SDM level is shown in fig. 6.3(b).

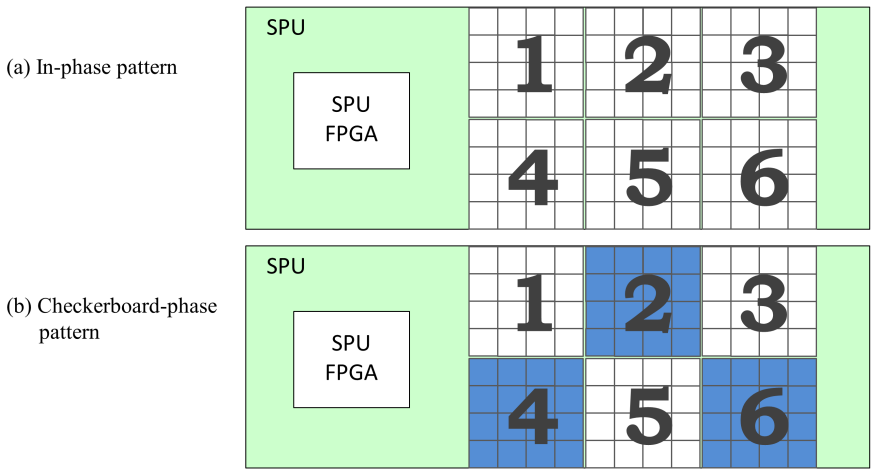


Figure 6.3: Phase pattern approaches at SDM level: Clocking all sensor dies of the SDM in-phase corresponds to the typical usage and thus is the reference scheme (figure (a)). A sensor die clock phase pattern with 180° phase shifts between complete stacks represents the checkerboard phase pattern at stack level scaled to SDM level (Figure reprinted from [148]).

For all measurements performed in the scope of this chapter, one SDM was used and configured to operate stand-alone with a direct connection to a control-PC as done for the measurements described in section 5.2.2. The only difference to the latter is that the stack FPGA firmware designs generate sensor die clock signals with a phase shift of 180° for a complete sensor tile in case of stacks 2, 4 and 6 (see fig. 6.3(b)) in addition to sensor die clock frequency shifts. Analogously to section 5.2.2, only stack-FPGA-internal logic and signalling between the stack FPGAs and the sensor tiles underwent shifts in clock phase. The remaining clocking of the SDM remained unchanged. Singles rate measurements with the SDM operated using the checkerboard phase pattern at SDM level were performed to ensure that the implemented phase shifting does not impair the SDM's data acquisition. The sensor die configuration, radioactive source as well as the singles processing procedure were kept identical to those described in section 5.2.2.

6.2.3 Characterisation

6.2.3.1 Field pattern measurements

To characterise modifications of the spatial EM field distribution emitted by the SDM as a function of sensor die clock phase pattern changes, the same lab bench setup was used as described under section 5.2.3.1 and shown in fig. 5.2. Using the magnetic field probe which was mounted on the XYZ-table enabling positioning in 3-D space, the magnetic field component of the EM field irradiated by the SDM was measured within lateral planes around the SDM (see fig. 6.4) in order to visualise the measurement positions of the planes as magnetic field maps. Field maps were acquired for the x and y components of the emitted $\vec{H}$ field for a frequency bandwidth of $\pm 100\,\mathrm{kHz}$ around the sensor die clock frequencies as listed under section 5.2.1. To cover the four lateral planes around the SDM, the field distribution of the left and top planes was measured, followed by a 180° flip of the SDM so that the former left and top plane became the right and the down planes. The field probe was moved 35 cm in x-, 10 cm in y-, and 9 cm in z-axis direction in steps of 5 mm which yielded 2769 measurement points. Thus, for all four planes, 5538 measurements were acquired. The field maps obtained with the checkerboard phase pattern approach were qualitatively compared to reference measurements resulting from sensor dies of all stacks clocked in-phase.

6.2.3.2 MRI noise measurements

The impact on the SDM-related noise coupled into the MRI RF receive chain when applying a checkerboard phase pattern at SDM level was evaluated analogously to section 5.2.3.2 using the SDM mounted without RF shield on the PET gantry, the mouse coil and the modified TSE sequence to perform noise scans with the clinical MRI system.

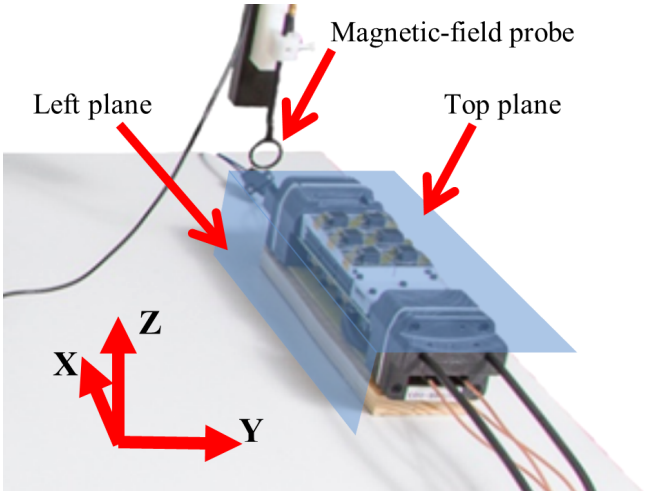


Figure 6.4: The SDM located on the lab bench setup as shown in fig. 5.2: The magnetic-field probe moves along the left and top planes in steps of 5 mm. The other two planes are covered by turning the SDM 180° with the detector stacks in direction and repeating the measurement (Figure reprinted from [148]).

6.3 Results

6.3.1 Simulations

As depicted in fig. 6.5, the MATLAB calculations of the magnetic field emission obtained with the 16 sensor dies oscillating in-phase yielded a single dipole field with a peak amplitude being in the order of magnitude of -3. Applying a checkerboard phase pattern resulted in a quadrupole field emission as seen in fig. 6.5(b). There, the order of magnitude of the four peak field amplitudes equals -7, being lowered by four orders of magnitude compared to the amplitude's magnitude obtained with the dipoles oscillating in-phase.

The FEM simulation results of the RF mouse coil and its screen are shown in fig. 6.6. The screen and the coil are excited by an RF field which originates from the dipole-modelled sensor tile for the case of in-phase clocking (figure (a)) and when clocked with the checkerboard phase approach (figure (b)). The vertical read arrows in front of the RF screen (recognisable as four small arrows actually being a 4×4 arrangement) represent the dipole emitters.

In fig. 6.6(a), the in-phase pattern results in a current distribution over the complete RF screen. This, in turn, leads to RF field coupling into the RF res-

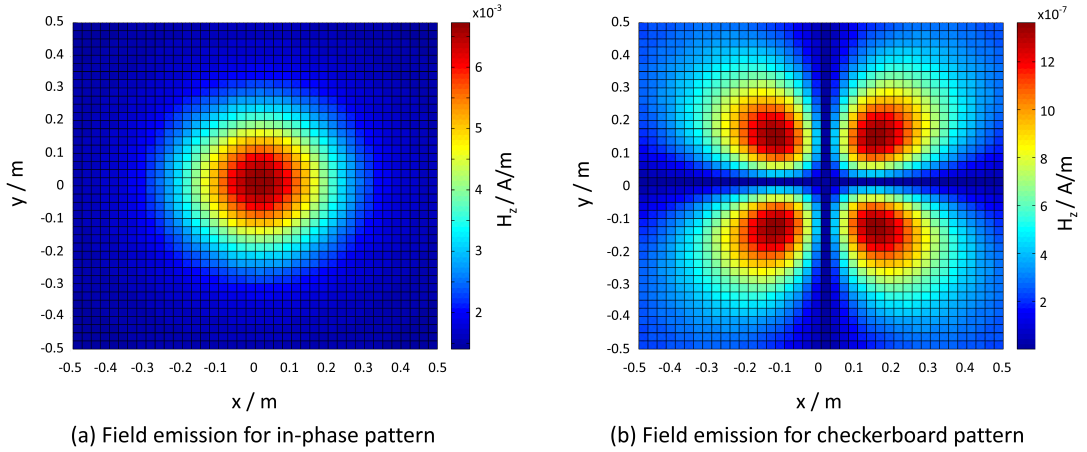


Figure 6.5: Field emission calculations of a sensor tile: In image (a) is shown the dipole field resulting from the in-phase pattern dipole oscillation. Image (b) depicts a quadrupole field generated when checkerboard-pattern clocking is applied. The difference between the peak amplitudes' order of magnitude of the two field emissions equals four (Figure reprinted from [148]).

onator with high efficiency which corresponds to strong spurious signal (noise) coupling from RF fields emitted by the modelled sensor tile into the MRI RF coil. In fig. 6.6(b), the application of the checkerboard pattern oscillation leads to a small excitation over the entire screen with a localised current distribution in front of the dipole model. Due to lower screen surface current amplitudes , the RF coil signal coupling is reduced. At red spots representing the highest current peak amplitudes, the difference between both simulation results is $-54\,\mathrm{dBA/m}$.

6.3.2 SDM operation

The single-SDM configuration was successfully operated with two different sets of stack FPGA designs yielding the in-phase and the checkerboard-phase pattern at SDM level at same sensor die clock frequencies. Singles rates at a clock frequency of 200 MHz were 119.7 kcps (standard deviation: 2.6 kcps) for the in-phase pattern and 120 kcps (standard deviation: 3.2 kcps) in case of the checkerboard pattern operation.

6.3.3 Characterisation

6.3.3.1 Field pattern measurements

In Figure 6.7 and fig. 6.8 are shown the field distributions (maps) measured for the four lateral planes of the SDM with the magnetic field probe for the x-component and the y-component of the emitted H-field, respectively. These fields maps were acquired while clocking the sensor dies with a clock frequency of 127.78 MHz. Figure 6.7(a) and fig. 6.8(a) depict the field maps obtained for the in-phase clocking, Figure 6.7(b) and fig. 6.8(b) represent the distributions for the checkerboard-phase pattern approach. The checkerboard-phase pattern approach yields modified magnetic field distribution and amplitudes compared to the in-phase pattern clocking when comparing qualitatively the figures (a) and (b) of a same H-field component.

6.3.3.2 MRI noise measurements

The MRI noise measurements obtained for the two different phase patterns with the clock frequency at 127.78 MHz, whose field distributions are presented in section 6.3.3.1, are shown in fig. 6.9. As the DPC sensor clock frequency was in this case equal to the Larmor frequency at 3 T, the noise distribution resulted in Lorenztian line shapes (see fig. 6.9(a)). The noise floor ratio of the measurement results lies in the range between 0.5 and 0.6.

6.4 Discussion

6.4.1 Simulations of the clock phase shift method

Generally, RF field emissions of electronic circuits are modified by changing the PCB layout regarding signal traces, by the choice of signal transmission standards (differential signalling compared to single-ended ones), by signal rise and fall times and by clock frequencies used for digital circuit operation. In addition, the field generation can be influenced when multiple digital components of a same type are identified and clock phase shifting is applicable to these components. This principle was illustrated by calculating an H-field distribution based on a model

of a sensor tile. The model was based on the assumption that the DPC sensors of the sensor tile combined with the single-ended signal traces connected to the sensors act as magnetic dipoles which emit fields upon periodic oscillation which represents the electrical periodic clock signal switching. Field distribution and amplitude calculations were done for the case of all dipoles of the tile oscillating in-phase being equivalent to the typical sensor tile operation. A second calculation was performed with adjacent dipoles of the sensor tile oscillating in opposite ways which corresponds to sensor die clock phase shifts of 180 ° being arranged in a checkerboard pattern. This configuration not oly led to a field distribution, but also to a magnitude reduction of the peak field amplitudes when compared to the in-phase-clocking-related calculation results shown in figure fig. 6.1. Due to the energy transfer between EM fields and a resonator being dependent on the coupling efficiency, modified RF field distributions obtained by clock phase schemes different to the typical in-phase clocking can help to reduce unwanted signal (noise) induction in the RF coil. This was demonstrated by the FEM simulations where the RF shimming and coil were excited by H-fields resulting from the in-phase and checkerboard-phase pattern of 16 dipoles representing a sensor tile. For the case of the checkerboard-phase pattern, the simulation revealed that signal intensities determined at the RF coil where five orders of magnitude lower compared to the intensities measured for the in-phase pattern simulations. However, as the FEM simulations only include a simplified sensor tile model and does not cover all EM field emission characteristics, these simulations in the first instance serve as a proof of principle.

6.4.2 Experiments

6.4.2.1 SDM operation

Similarly to the results obtained in section 5.3.1, the SDM successfully acquired PET data when operated with the checkerboard-phase pattern at SDM-level. However, for the scope of the field distribution and the MR noise studies, the single-SDM operation served primarily the purpose in the scope of the lab bench field map and MRI noise measurements to irradiate RF fields. Regarding the PET singles processing, any parameters related to it were not affected by the modified clock phase pattern scheme at SDM level, as singles are clustered per

entire sensor tiles with all sensor dies being in-phase at sensor tile level. In case of PET prompts detection for data acquired with a PET detector which operates with clock phase shifting with an impact on time stamping of hit data, the clock phase differences need to be taken into account for the PET coincidence processing. If opposite detectors acquire PET hit data with a clock phase offset leading to hit data time stamp shifts, the offsets need to be corrected in order to avoid uncorrelated PET singles to be detected as true coincidences and vice versa. In case of the Hyperion II^D platform, either a time stamp offset correction could be performed within the SDMs during PET data acquisition, or it could be done later during the offline singles or coincidences processing. Sensor die clock phase shifting at sensor tile level would require time stamp corrections prior to Singles clustering as ,depending on cluster critera, incomplete clusters of hit data might result which leads to higher hit data rejection ratio (lower singles rate) and inaccurate singles positioning when the detector does not use one-to-one coupling between scintillation crystals and sensors.

6.4.3 Characterisation

The field maps acquired with the lab bench setup while the SDM operates with sensor tiles clocked in-phase and with the checkerboard-phase pattern reveal differences in the field distribution related to the modified clock phase pattern. Particularly the top planes of figs. 6.7 and 6.7 being those facing the sensor tiles show differences between in-phase and checkerboard phase pattern schemes in terms of spatially shifted amplitude peaks with similar amplitude values. As the clock phase pattern change at sensor tile level led to a modified coupling efficiency in the FEM simulations, an influence on the noise signal coupled into the MRI RF coil using the checkerboard pattern at SDM level was anticipated. The MRI noise measurements confirmed these expectations as shown in fig. 6.9.

6.5 Conclusion

This chapter presented an RF interference reduction method dealing with clock phase modifications of digital, clocked circuits of PET detectors. Investigations covering simulations, lab bench and MRI noise measurements were performed

to analyse the proof-of-concept and first results confirmed that modified clock phases can lead to optimised RF emission distributions to reduce the coupling efficiency between PET-detector-related RF fields and the MRI RF coil to reduce the induced noise. As next steps, further simulations and measurements using the complete insert should be done in order to optimise the field distribution in order to effectively reduce the noise coupling to a minimum.

6.6 Overall conclusion on the interference reduction techniques presented in chapters 4 to 6

The RF interference reduction technique called RESCUE (crefchap:RESCUE) aims at the preservation of the MR image quality by interrupting the PET data acquisition during MR RF receive phases. An interrupted PET data acquisition leads to less prompts available for PET image reconstruction. Preserving the MR image quality using RESCUE therefore occurs at the expense of the PET image quality, if the PET/MRI examination protocol does not take into account a longer PET data acquisition to compensate for the prompts not recorded due to interrupted PET during the MR RF acquisition phases. The higher MR RF acquisition duty cycle, the smaller the PET data acquisition duty cycle, which is why RESCUE is not suited for MR protocols including sequences such as gradient echo sequences with high RF acquisition duty cycles and echo planar imaging. Compensating the prompts missed during MR RF acquisition phases by prolonging the PET measurement when comparing to an uninterrupted PET scan also implies, that dynamic PET scans should be avoided when applying gated PET scans using RESCUE. As its name suggests, this technique was introduced to offer the possibility of reducing PET-related noise coupling into the MR receive chain when new MR sequences, MR coils, or a combination of both are applied that result in a high sensitivity towards PET-related RF noise and thus degrade the MR image quality. Such a use case may particularly apply to simultaneous PET/MRI employed in research-driven environments, e.g. PET/MRI protocol or drug development. In case of unsatisfactory RF shielding of the PET electronics which may also lead to RF-leakage - something which may happen when working

with PET detector prototypes - RESCUE may also serve well its purpose, as RF shielding development and its production are usually costly and time-consuming and thus cannot be replaced or modfied that easily once the PET detector is completed.
Solutions to the MR-based synchronisation needed to start and stop RESCUE were presented either by modifying MR sequences to generate triggers via the MRI back-end to be fed into the PET synchronisation unit, or to use signaling provided by MRI RF transmit/receive coils. The former requires knowledge about MR sequence pulse programming which is not available at every PET/MRI site which is why the latter solution would be preferable, as it may not need to modify MR sequences. However, knowledge provided by the RF coil manufacturer regarding the coil transmit/receive electronics would be required to interface the electronics with the PET subsystem.
In contrast to RESCUE, the interference reduction techniques presented in chapters 5 and 6 aim at a continuous PET operation during MRI operation while reducing PET-related noise emission coupled into the MRI RF receive chain. These techniques address digital, clocked electronics, as these are particularly prone to RF emission due to periodic signal switching often using steep signal slew rates. Depending on the electronic components located within or in proximity of the MRI bore, their clock frequency can be shifted to lower or higher frequencies in such ways that the emitted spectra result in lower signal amplitudes in the frequency ranges, the MRI RF receive chain is sensitive to. This reduces the coupled noise. Similar to the frequency shift, a phase shift between electronic components of same clock frequencies can lead to a modification of the emitted spectra. The spatial change in emitted fields demonstrated in chapter 6 by applying a 180° phase shift between adjacent sensors as well as between adjacent detector stacks (checkerboard pattern) resulted in reduced noise coupling.
The clock phase shift approach may be suitable for PET electronics where several to many components of a same type with an influence on the EM field emission can be identified. It needs to be taken into consideration, that an introdcued clock phase shift does not alter the aimed, operational behaviour obtained with their components and their spatial arrangement on the printed circuit boards. Shifting the clock frequency can in principle be applied to any digital, clocked component. Those that have a high fraction in emitting noise should be identi-

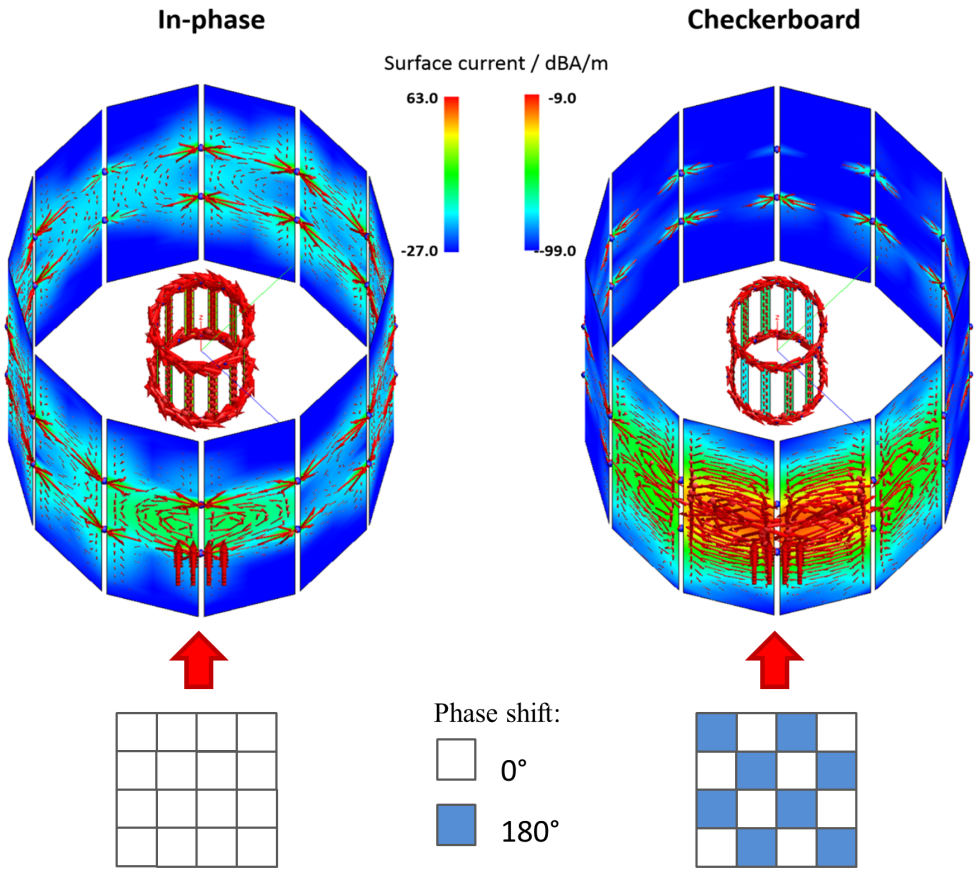
fied and then analysed with regard to possible frequency shifts in order to again modify the overall emitted field spectra. If such components have an influence on the data acquisition bandwidth, then the resulting consequences with regard to a reduced PET data acquisition bandwidth in the case of a lowered frequency or bottlenecks potentially introduced behind components with raised frequencies need to be considered. In chapter 5, the DPC sensors themselves where clocked with lower frequencies to reduce the emitted noise. In this case, the MRI SNR preservation occurs at the expense of a reduction regarding the maximum therotical PET data acquisition bandwidth. Here, it needs to be considered if the resulting lower maximum prompts rate limits an aimed PET scan. Particularly the clock and phase frequency techniques could help to optimise the emitted RF fields in such ways that the RF shielding can be reduced to a minimum or even be omitted. That is of particular interest for PET detectors being closely located to the RF coil field-of-view in order to reduce any MR image artefacts related to magnetic field distortion introduced by shielding. In case of the Hyperion II^D architecture, the clock frequency and phase shift techniques as well as RESCUE where applied at PET module level by solely modifying firmware that can be reprogrammed at any time in the field. This allows flexible adaptations of the PET-related field emission when e.g. different and new RF coils are operated with the same PET detectors.

Important to underline is that all three techniques are not limited to the DPC sensor. Although the latter was used to study the three presented techniques, they are also applicable to any digital, clocked components used in PET detectors, including analogue SiPMs and APDs combined with mixel-signal ASICs, and e.g. any type of DACs, ADCs and FPGAs.

Conventionally, PET-related RF interference reduction for simultaneous PET/MRI imaging has been achieved by applying RF shielding materials as presented and discussed in detail in section 4.1. Besides possible MRI magnetic field distortion close to RF shields of PET detectors, a disadvantage of shielding is the lack of flexibility once the EPT detectors are installed. In constrast, RESCUE may be used optionally depending on the needs and adapts dynamically to the MRI RF acquisition duty cycle. The techniques making use of clock frequency and phase shifting were demonstrated by solely modifying FPGA firmware code of the PET detector which can be reprogrammed at any time in the field. Such flexible ap-

proaches would allow to optimise the RF interference reduction when different MRI RF coils are used with a same PET detector, or when the latter is combined with different MRI systems. To my knowledge, approaches with such a flexibility as presented in chapters 4 to 6 were the first ones to be proposed in the scope of PET-related RF interference reduction methods.

As a next step, the three techniques need to be evaluated at PET system level. In case of RESCUE, the MRI-based synchronisation needs to be implemented either at RF coil at MRI system back-end level in order to evaluate a synchronised operation of the PET detectors with the MRI. In case of the clock shifting techniques, MRI SNR measurements need to be performed with and without the PET modules' RF shielding in order to study the influences on the PET-related RF noise coupling. This study shoul also yield in optimal frequencies and phase-shift combinations for the DPC sensor clocking used in Hyperion II^D.



(a) In-phase pattern

(b) checkerboard-phase pattern

Figure 6.6: Simulated surface current distribution results: In figure (a) the RF field resulting from an in-phase pattern dipole oscillation yields noise coupling into the coil with high efficiency. Image (b) visualises the checkerboard-pattern-related field emission leading to a reduced coupling efficiency (Figure reprinted from [148]).

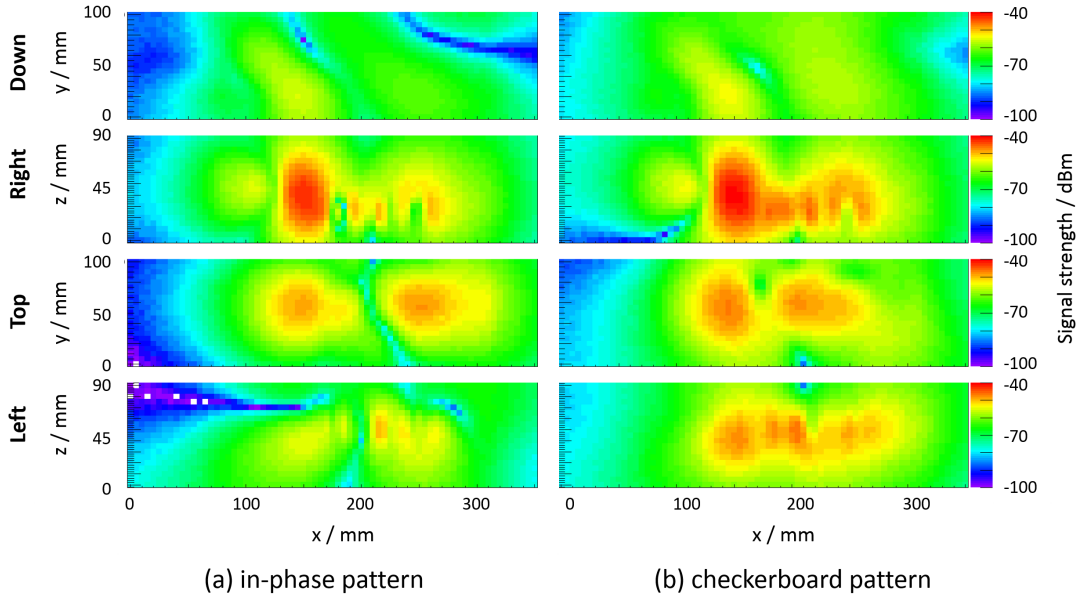


Figure 6.7: Field maps for the x-component of the emitted H field obtained for clocking at 127.78 MHz with in-phase pattern (a) and checkerboard-phase pattern (b) at SDM level (Figure reprinted from [148]).

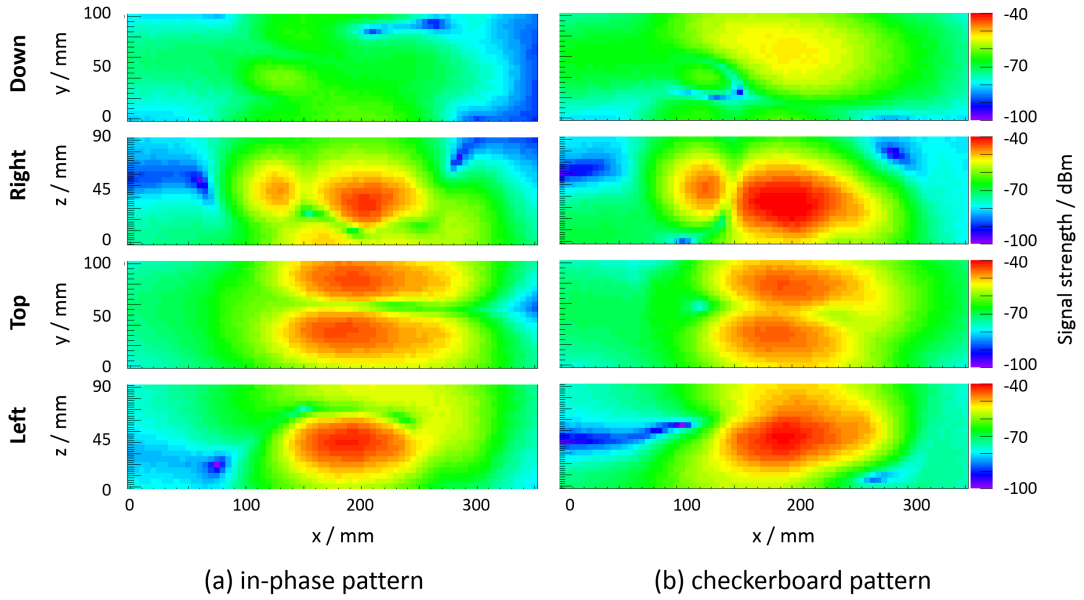


Figure 6.8: Field maps for the y-component of the emitted H field obtained for clocking at 127.78 MHz with in-phase pattern (a) and checkerboard-phase pattern (b) at SDM level (Figure reprinted from [148]).

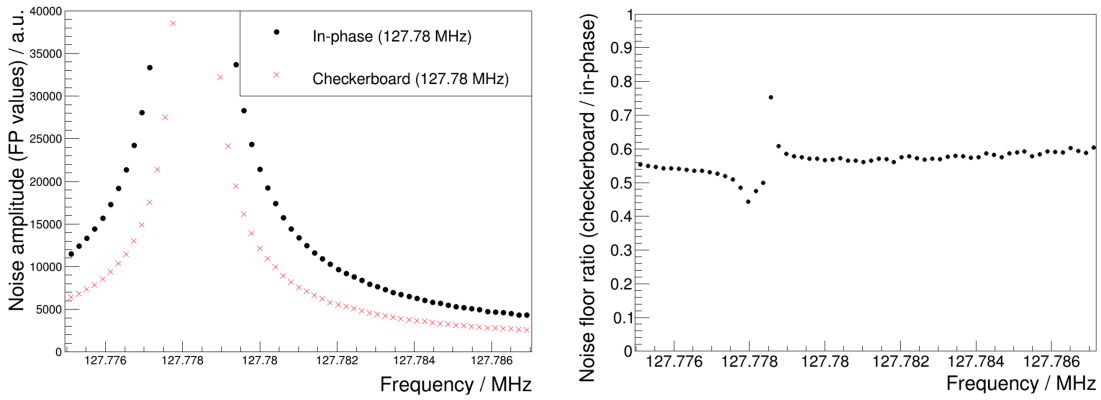


Figure 6.9: Figure (a): MRI noise measurements at a sensor die clock frequency of 127.78 MHz for cases of in-phase and checkerboard pattern applied at SDM level. Figure (b): noise floor ratio of noise results shown in figure (a) (Figure reprinted from [148]).

Chapter 7

Demonstration of the Hyperion II^D system

All in all, three Hyperion II^D prototype systems were built of which one is located at King's College London (KCL) [1].

[1]The measurements were performed in the Department of Biomedical Engineering which is part of the Division of Imaging Sciences and Biomedical Engineering (within the Faculty of Life Sciences and Medicine)

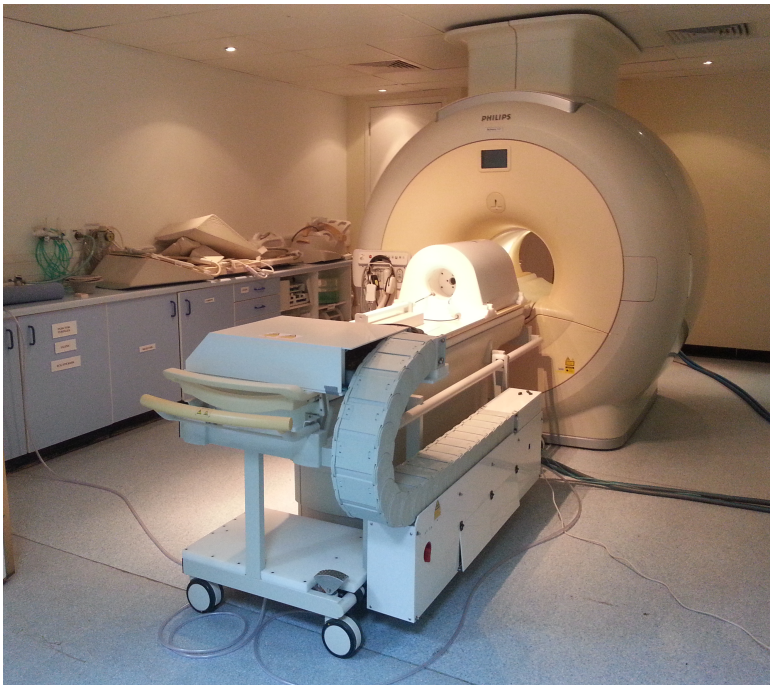


Figure 7.1: The PET insert placed in front of the 3-T MRI (Philips Achieva 3T) and ready for simultaneous PET/MR imaging.

This chapter gives a brief overview on *in vivo* and *in vitro* PET/MR imaging results obtained from measurements at KCL that were done by myself to demonstrate the imaging capabilities of the system. The insert installation in the MRI examination room is shown in fig. 7.1. A holder (PET bed) was constructed as a pipe to fit into the bore of the RF mouse coil. Figure 7.2 depicts the holder with a mouse under anaesthesia. It was designed in such a way that it has an open space to place the subjects to be scanned in it. Both ends of the holder are open to pass cabling and tubes for respiratory gating, electrocardiogram (ECG) signals and anaesthetics in case for *in vivo* imaging.

7.1 Bone PET/MR imaging

The very first Hyperion II^D *in vivo* PET/MR images were acquired by performing a mouse bone-scan using sodium-fluoride (^{18}F-NaF) as the PET tracer. The tracer was administered half an hour before the imaging procedure began. At measurement start, the tracer activity was 19.9 MBq. For MR imaging, a 3D T_1

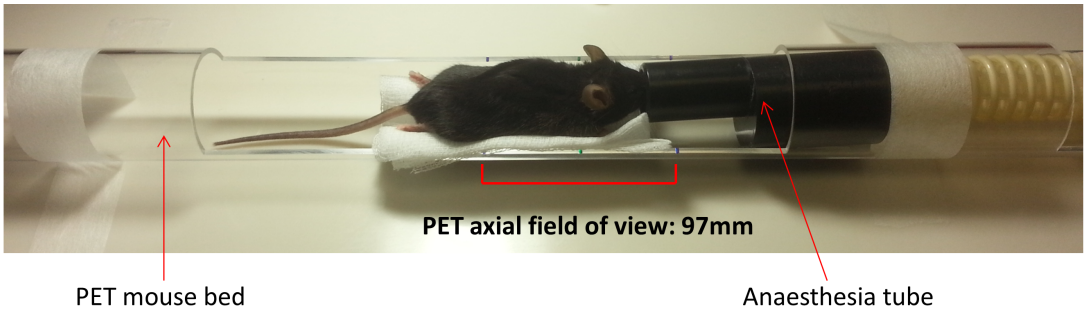


Figure 7.2: PET bed with the mouse under anaesthesia. The region of interest to be scanned with PET is placed in the axial FOV centre where the sensitivity is highest.

weighted gradient echo sequence (voxel size: $0.25x0.25x1.00\,\mathrm{mm}^3$, ROI acquisition time: 5min) was chosen. PET data was acquired during 9 minutes during which 256 Gbytes of raw data were processed to yield 125.29×10^6 coincidences. The PET images were reconstructed using maximum-likelihood-based OS-EM (voxel grid: 200x200x387 voxels with 0.25 mm pitch). The MRI scan was performed simultaneously with the PET scan. The PET/MRI results are shown in fig. 7.3. Figure 7.4 shows coronal and sagittal views of the bone scan. The delicate structures of the murine vertebrae and ribs can be clearly distinguished.

7.2 Cardiovascular PET/MR imaging

In the department of biomedical engineering, research in done amongst others in the area of *cardiovascular diseases* (CVD). The research group led by Prof. Ren Botnar which focusses on novel MR sequences and contrast agents for cardiovascular imaging investigates in the early detection of atherosclerosis by imaging plaques with non-invasive imaging techniques. More background and details can be found in [173] and [174]. The group uses high-resolution MRI (approx. 0.1 in-plane pixel resolution) to image atherosclerotic plaques in mice and has begun investigating hybrid PET/MR imaging which could offer advantages thanks to the higher sensitivity of PET compared to MRI. To evaluate the suitability of the PET insert for cardiovascular PET/MR imaging of mice, preliminary measurements were performed and the imaging results are presented below.

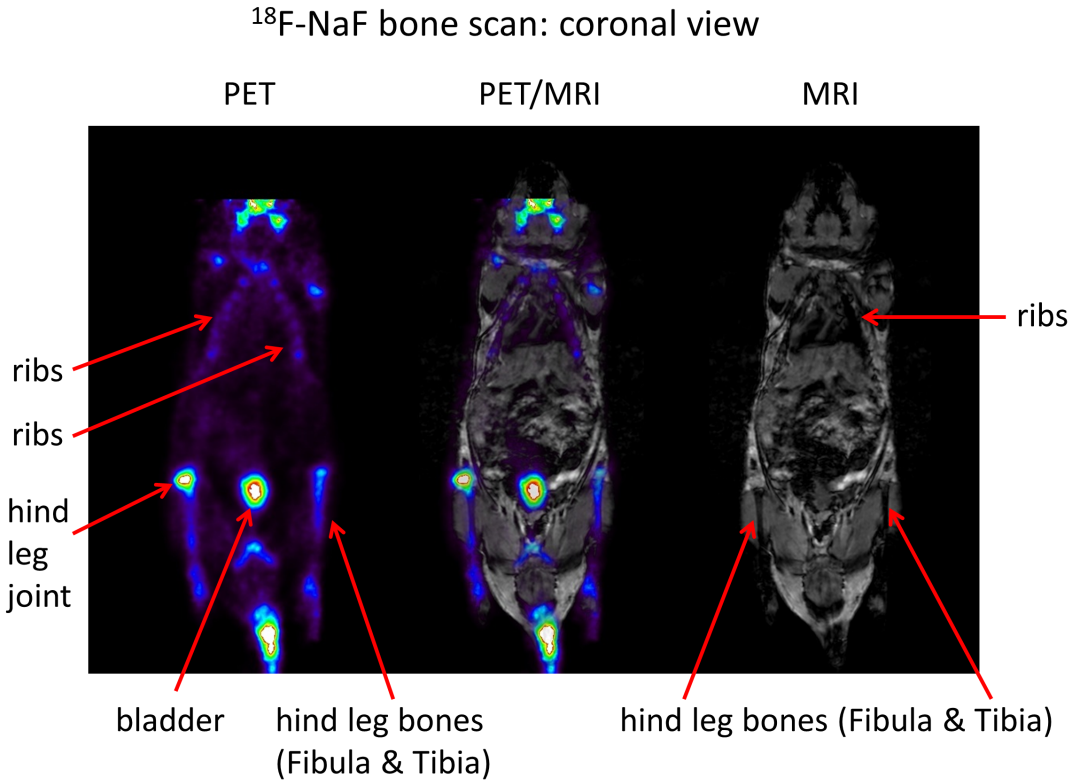


Figure 7.3: PET/MRI bone scan results: The ribs and the hind leg bones and joints are clearly seen.

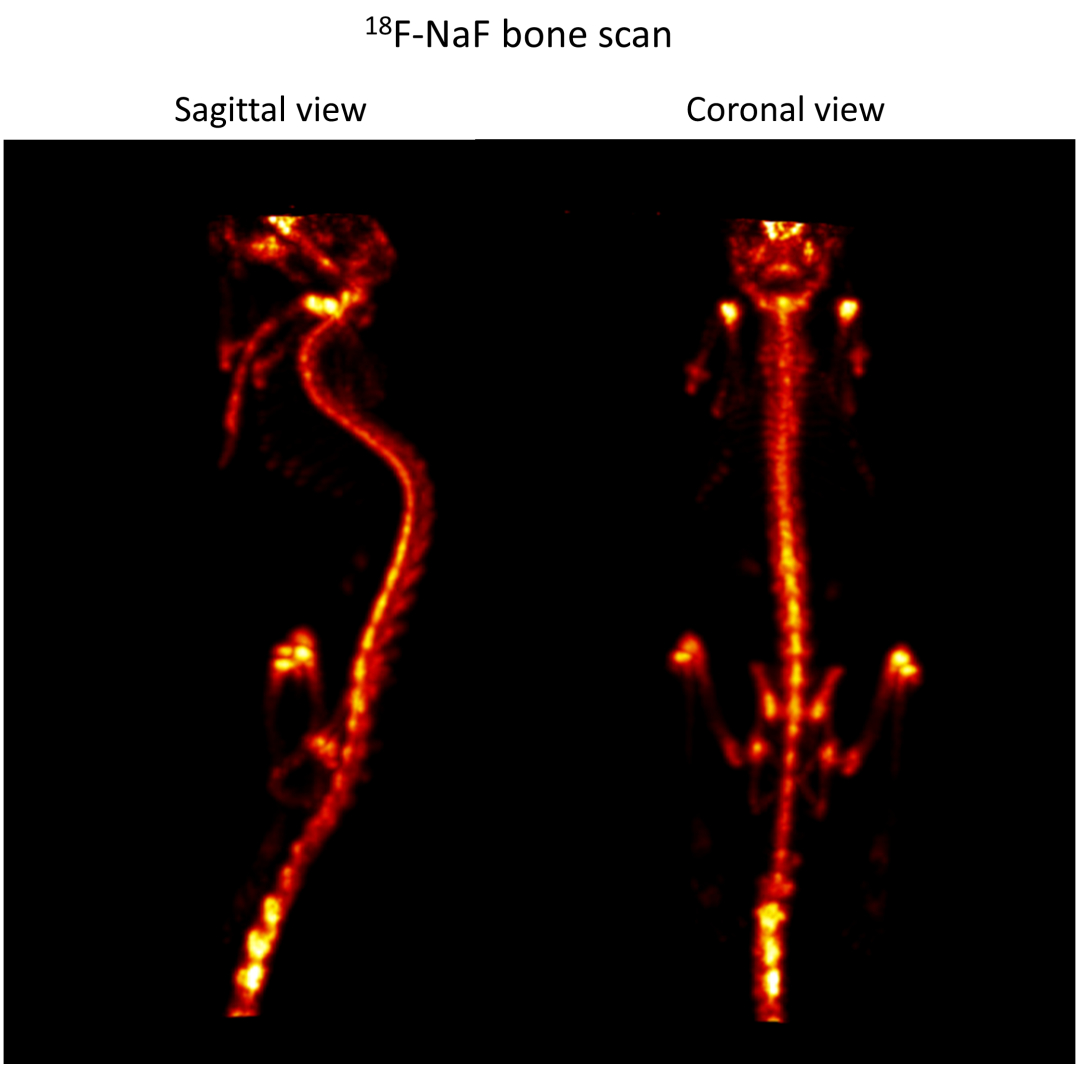


Figure 7.4: PET bone scan: The vertebrae and the ribs are well resolved in the images.

In the field of atherosclerosis research, murine models of type APOE$^{-/-}$ are commonly used as they develop substantial plaques particularly in the vessel walls of the aortic arch and the brachiocephalic artery (BCA) when they are fed with a high-fat diet for a period of approx. 12 weeks. The location of the BCA and the aortic arch are shown in fig. 7.5. Plaques in the BCA and aortic arch are typically imaged in transverse slices (planes).

A first evaluation with PET was done by injecting a ^{64}Cu-labelled elastin-binding contrast agent (ESMA) in a control animal, i.e. an animal without plaque formation. ESMA binds to elastin, an extracellular matrix protein residing

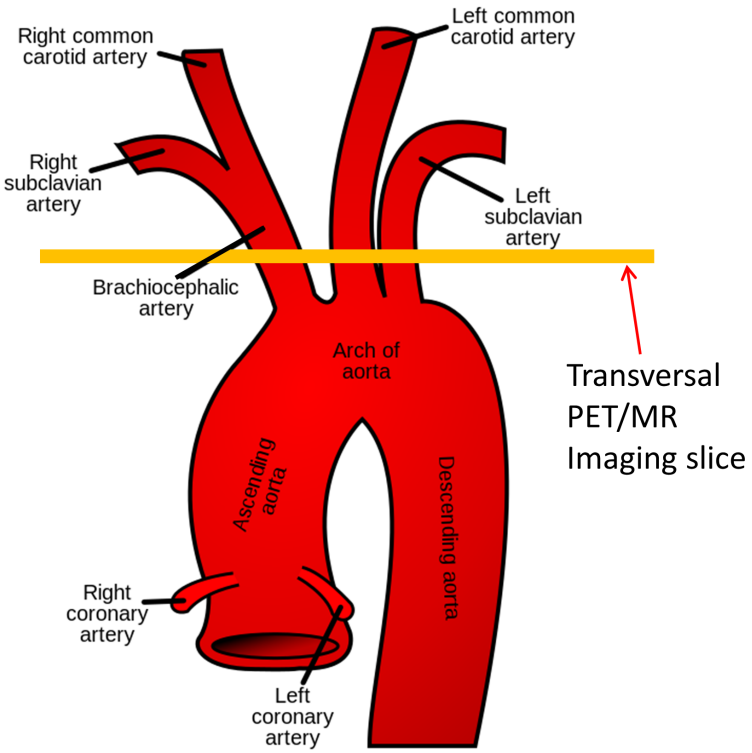


Figure 7.5: Overview of the aortic arch and its outgoing arteries. For plaque imaging of the brachiocephalic artery (BCA), PET/MR images of the transversal slice through the BCA, left carotid- and left c. subclavian arteries are acquired (Figure adapted from [175]).

in arterial vessel walls. ESMA therefore should accumulate in the aortic arch, BCA, left carotid and subclavian arteries. One hour after the injection of the tracer into a murine control animal, PET data was acquired for 24 minutes with a radionuclide activity of 24 MBq at the start of the measurement. A 3D MRI angiography scan was performed to visualize the arterial and aortic lumen. The resulting transverse PET/MR images are shown in fig. 7.6. One transverse slice depicts the arch, whereas the other slice shows the the arteries which are outgoing from the arch. Given their small dimensions (0.5 mm in case of the BCA), the vessel walls cannot be separated from the lumen, but the three arteries are easily distinguishable. The PET signal intensities of the BCA and the left carotid artery are comparable with the left subclavian artery being less intense.

Encouraged by the promising PET/MR images, a diseased animal with plaques

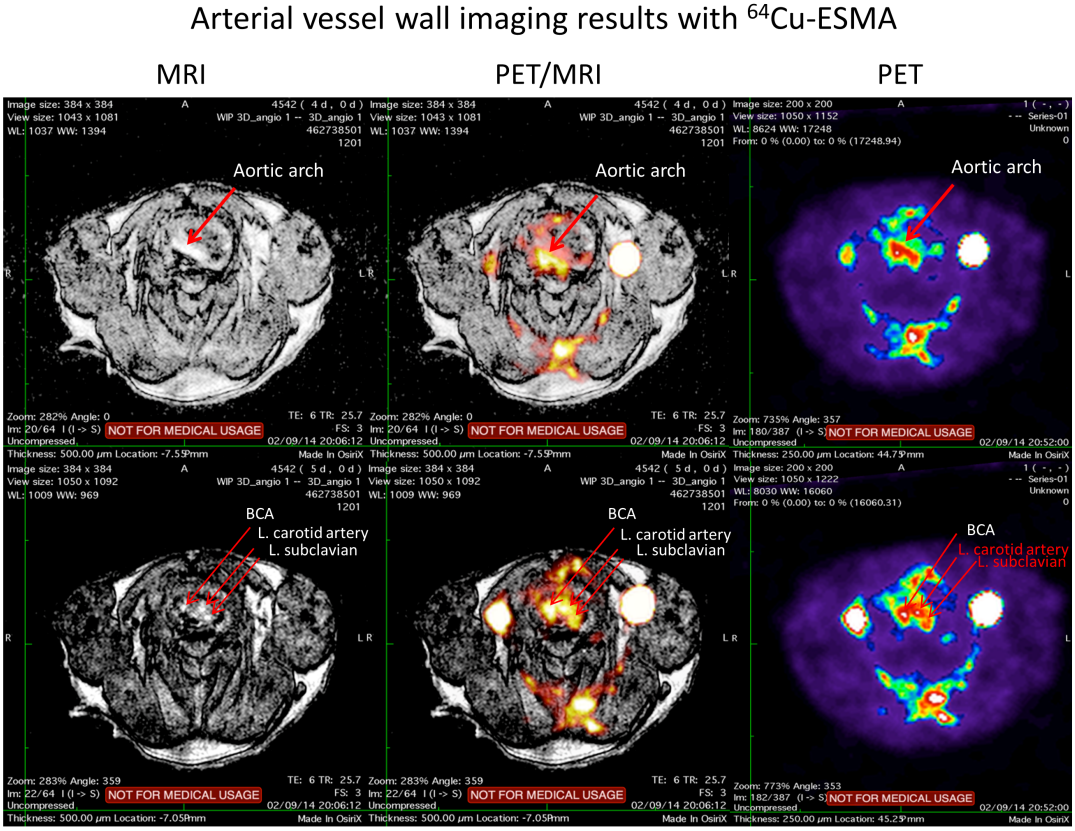


Figure 7.6: Vessel wall imaging results of the aortic arch, the brachiocephalic- (BCA), left carotid- and left subclavian arteries using a ^{64}Cu-labelled elastin-binding contrast agent (ESMA). The three arteries of the mouse (control animal) are visible in the PET image.

was imaged as a next step. An an APOE$^{-/-}$ mouse with 11 weeks of hi-fat diet and plaque formation in the BCA and the arch was injected with ^{64}Cu-ESMA. After two hours of tracer uptake time (typical uptake time of ESMA), PET images were acquired for 33 min with a tracer activity of 19.78 MBq at measurement start. MRI images were acquired using a 3D angiography sequence. In fig. 7.7 it can be seen that the PET signal is stronger in the BCA compared to the other two arteries. This is related to the higher ESMA-uptake by the plaques located in the BCA.

In order to evaluate the PET insert for rabbit imaging of atherosclerosis, initial *in vitro* experiments were performed in order to determine, if rabbit-sized arterial

vessel walls can be distinguished from the vessel lumen. For these measurements, a piece of abdominal aorta from a rabbit with one plaque in the vessel wall was soaked for two hours in ^{64}Cu-ESMA with an activity of 12.4 MBq diluted in saline. Afterwards, the aorta was rinsed several times and the activity of the bound tracer was measured to be 1.3 MBq. The aorta was then attached to cork and the cork with the aorta was inserted in a falcon tube filled with saline, as shown in fig. 7.8.

The PET measurement time was 1.5 h to acquire sufficient data at the low tracer activity (340 Gbytes of PET raw data yielding 52×10^6 coincidences). MR images were acquired using a 3D T_1 weighted TSE sequence (resolution: (0.25x0.25x0.5) mm^3, Tr= 1000 ms, TE = 11 ms, acquisition-matrix: 240x160, acquisition-resolution: (0.25x0.25x0.5) mm^3, flip angle: 90°, TF: 16, acquisition time: 22 min) for coronal and transverse images. Figure 7.9 depicts coronal views of the abdominal rabbit aorta. The plaque shows very little uptake possibly due to a fibrotic core. This is still under investigation. However, the images reveal a separation from the lumen and the vessel wall in the PET image. The lumen diameter is approx. 2 2mm and 1.65 mm at the plaque location.

Figures 7.10 and 7.11 are transverse image slices of the aorta at the plaque location and a vessel wall location with higher uptake, respectively. Both images demonstrate that the PET image resolution allows clear separation of the lumen from the vessel walls.

Summarised, these initial image results demonstrate the PET insert's capabilities in the field of small rodent imaging. However, further investigations are needed to study the imaging capabilities when performing scans of larger animals (i.e. rabbits). This would serve as a prerequisite study for future *in vivo* PET/MR measurements of rabbits with atherosclerotic plaques.

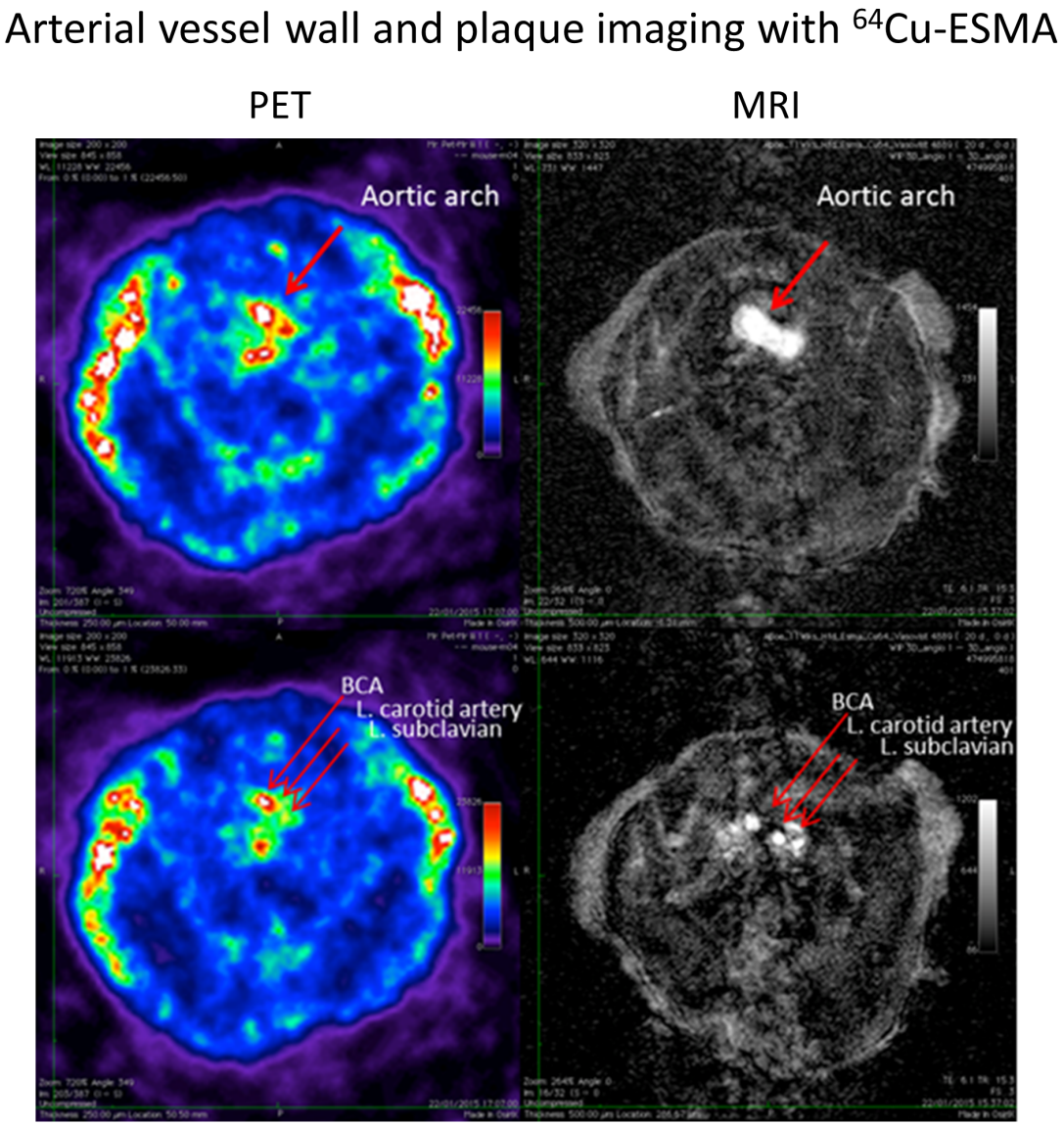


Figure 7.7: Vessel wall imaging results of the aortic arch, the brachiocephalic- (BCA), left carotid- and left subclavian arteries from an $APOE^{-/-}$ mouse with atherosclerotic plaques in the BCA using a ^{64}Cu-labelled elastin-binding contrast agent (ESMA). The PET images shows significantly higher uptake in the BCA compared to the carotid and the left subclavian arteries.

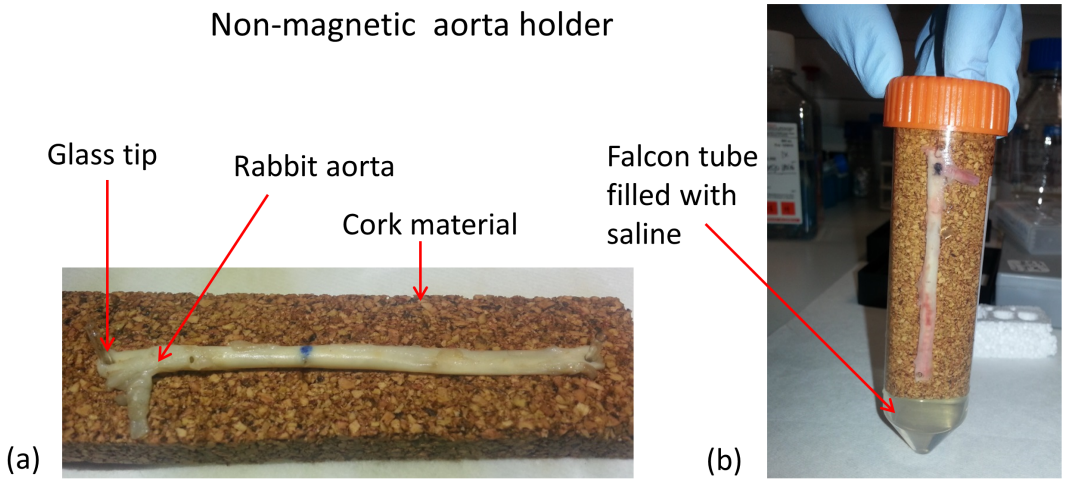


Figure 7.8: Image (a) depicts the piece of abdominal aorta fixed to the cork material. Image (b) shows the Falcon tube filled with saline and the piece of aorta inside.

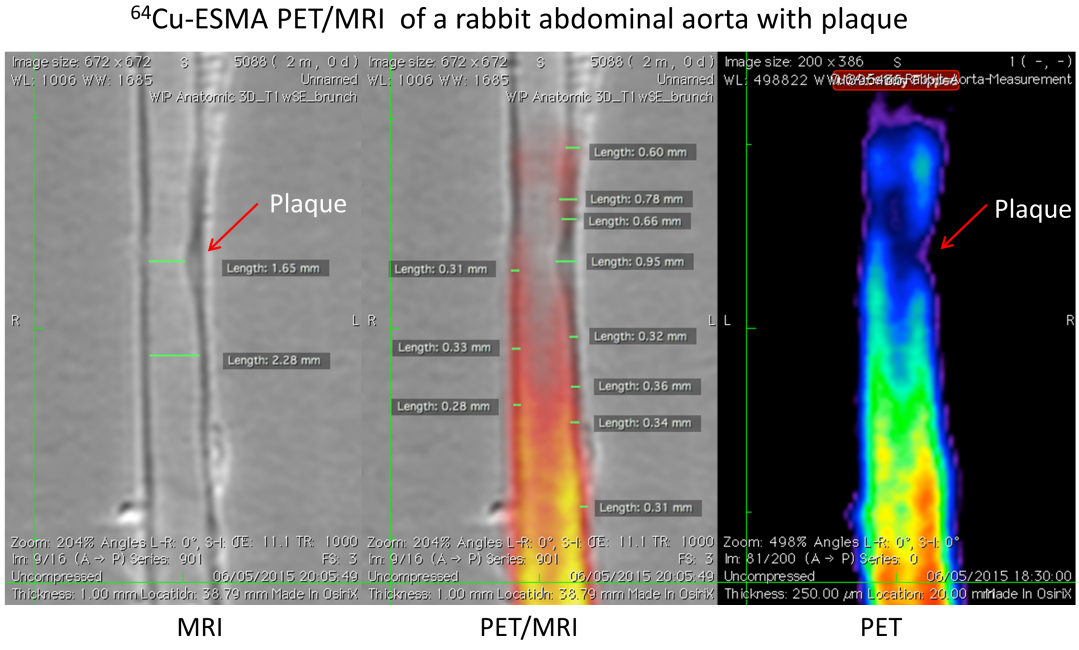


Figure 7.9: Coronal images of the rabbit aorta. The plaque shows little to no ESMA uptake. The vessel wall can be separated from the lumen in the PET image.

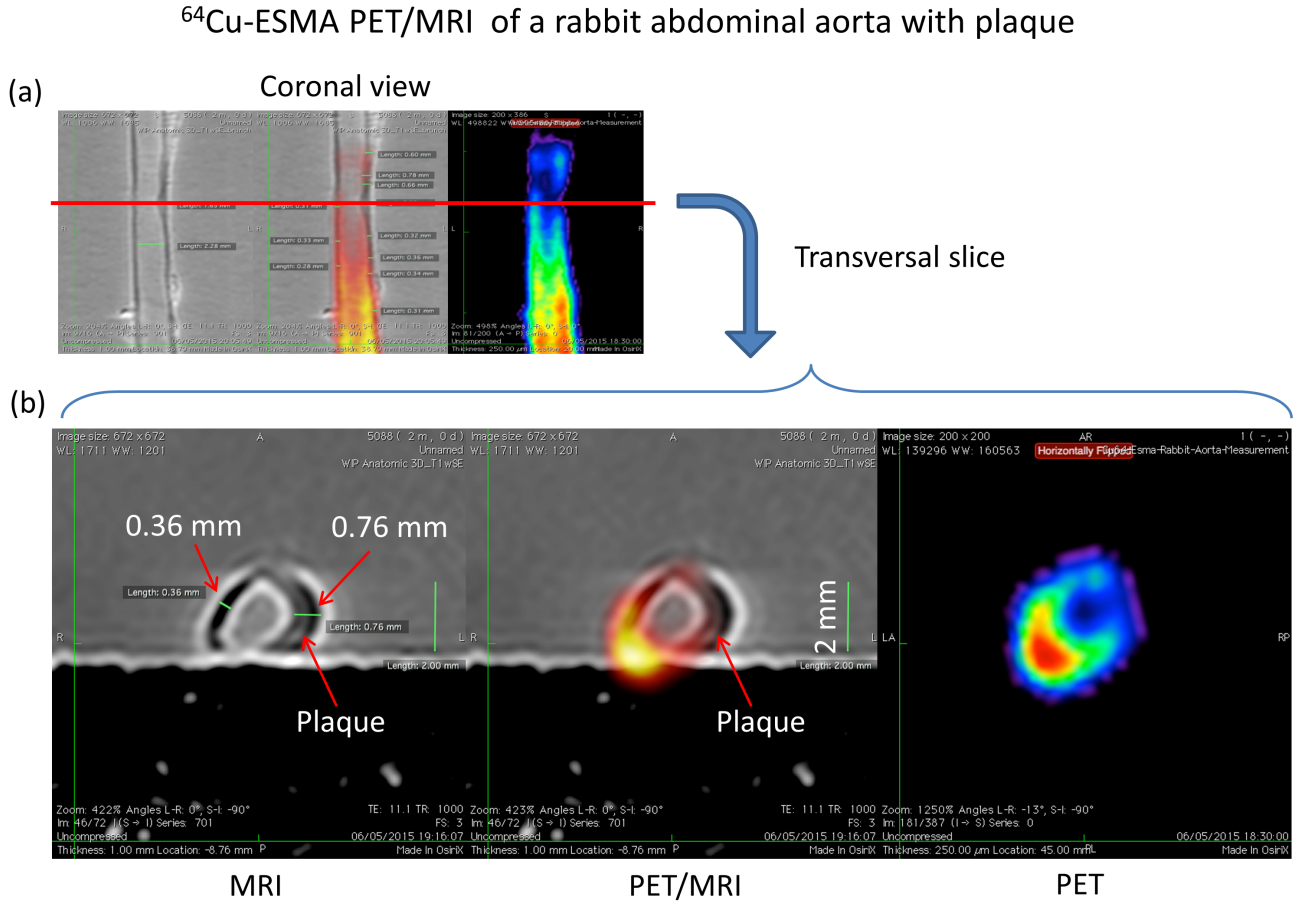


Figure 7.10: A transverse slice of the aorta was scanned at the position of the red line as shown in figure (a). The plaque does not show any PET tracer uptake. However, the the vessel lumen can be separated from the PET tracer uptake in the vessel wall opposite to the plaque location.

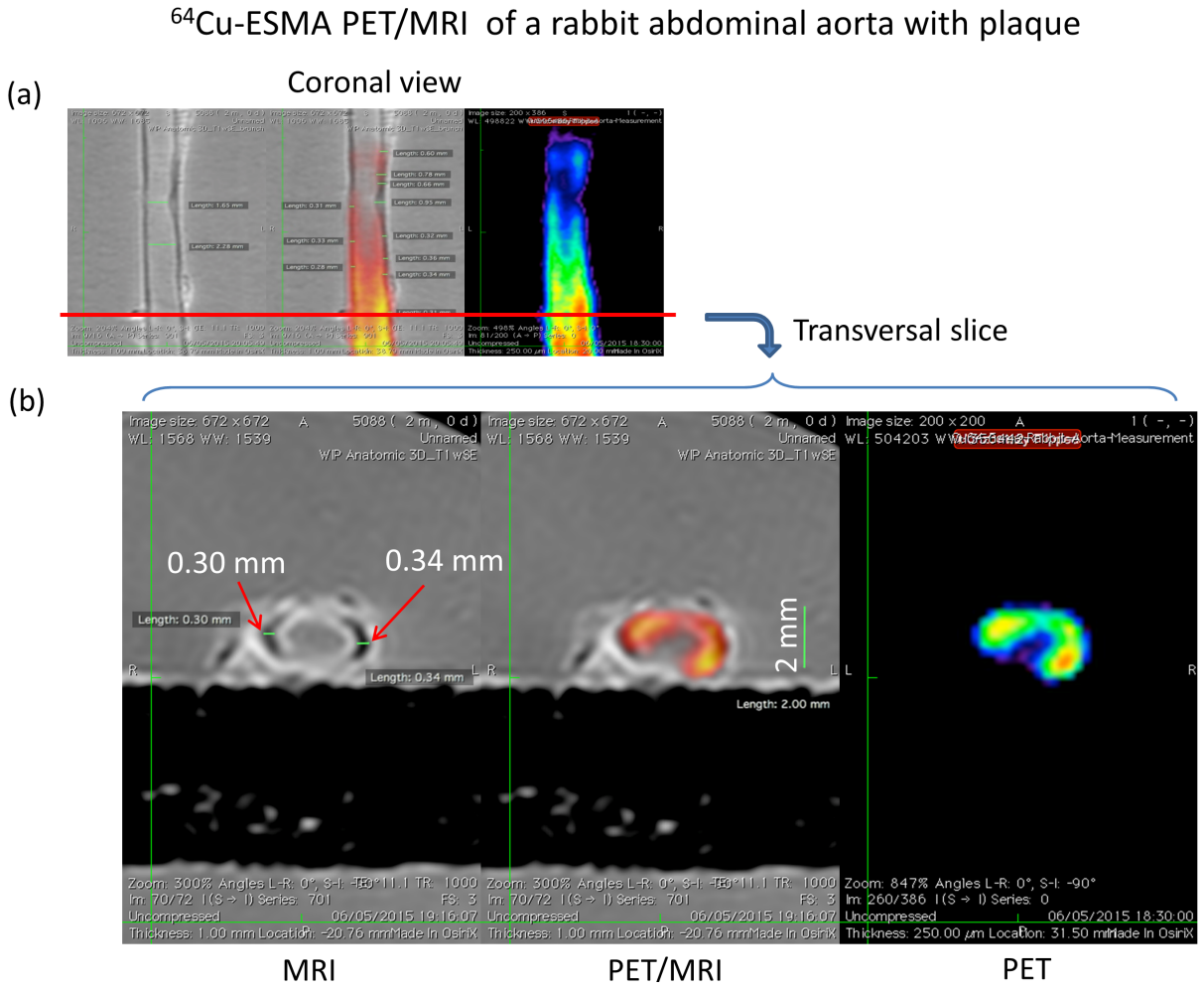


Figure 7.11: A transverse slice at the position of the red line (figure (a) of the aorta at a position with high uptake is shown in figure (b). The vessel lumen is cleary distinguishable from the vessel wall.

Chapter 8

Conclusion

The technological advancements in the field of photo-detectors - namely the rise of APD, SiPM and dSiPM sensors - enabled the breakthrough in integrating PET detectors into MRI systems to allow for truly simultaneous PET/MR imaging with an increasing hybrid PET/MRI FOV while offering an acceptable PET performance. Furthermore, silicon photo-multiplier technology offers response times and signal gains comparable to those of conventional photo-multipliers, thereby making TOF-PET possible for PET/MRI which corresponds to the state-of-the-art performance of PET/CT systems. As semiconductor sensors are designed with small sizes in the range of a few millimetres, a direct one-to-one coupling between the sensors and scintillation crystals can be achieved for clinical systems which further improves the PET system performance. With the small detectors facilitating densely packed detector designs, new detector configurations for imaging instrumentation for nuclear medicine can be explored which is an area of ongoing research. However, the smaller the photo-detectors are, the more the number of detector channels increases when considering a similar detector area. This leads to an increasing number of detector data channels to be acquired and processed in parallel. As an example, the difference in the channel number between the PMT-based *Gemini TF* with 420 channels and the dSiPM-based *Vereos* with 23040 channels (both are clinical PET/CT systems from Philips) is two orders of magnitude. The first aim of this thesis was to develop a PET data acquisition architecture suitable for current and future types of PET detector configurations, and for all application areas (preclinical, brain-imaging, clinical). To realise a "one-fits-all" approach, the architecture is based on con-

cepts that provide for a high degree of scalability and flexibility with regard to the data acquisition topology and the type of node (software- or hardware-based implementations). Topology-wise, a tree-topology with daisy-chain links between nodes at a given tree level was adopted. An application-layer-based communication protocol was conceived to support acquisition platform designs with flexible combinations of software- or hardware-based nodes and that was independent of the type of inter-node communication link. As the protocol includes a modular addressing scheme and the inter-node communication is performed via the store-and-forward principle, there is virtually no limit on the number of nodes and hence the number of detector channels that can be accommodated. Concepts that ensure quality-of-service and robustness of communication were presented in chapter 3 that were able to avoid congestion or regulate it in controlled ways, and identify and discard corrupt or missing data messages. The differentiation between detector data messages and control- and status-data messages introduces the possibility of prioritising these variably depending on latency-related requirements (e.g. for distributed PET coincidence processing) or on changes in fractional throughput usage. All nodes follow the same principles of data message decoding/ encoding, and the same communication interfaces for node-internal data processing modules. This allows the use of same node-internal modules over multiple nodes to allows processing tasks to be distributed. This modular concept applies to software-based as well as to hardware-based nodes. The modular protocol addressing structure offers a modular design approach for message protocol encoders and decoders, thereby enabling efficient software or firmware code reuse. All data message types can be sent over single, shared links between nodes which reduces costs, mitigates the probability of electrical, optical or mechanical interconnection problems, eases maintenance-related works, and allows for higher system integration. The latter three points are important criteria for highly integrated PET detectors designed to operate in an MRI system.

These architectural concepts are all of general nature and are generically applicable regardless of the type of communication-link or node. This permits a large variety of different implementations depending on the needs and aims of any target PET and PET/MRI system. The very high degree of flexibility and modularity is to a large extent attributable to the protocol structure which has, to my knowledge, not been previously reported in literature.

The proposed data acquisition architecture was implemented for both the preclinical Hyperion I and II^{D} PET systems, which are SiPM/ASIC- and dSiPM-based inserts for simultaneous PET/MR imaging using a clinical MRI. In chapter 3, the data acquisition platform for Hyperion II^{D} was presented, and the data transmission behaviour over the entire throughput range was investigated using data generators located at the data acquisition front-end. No data loss or corruption was observed up to the point where messages are intentionally discarded at rates beyond the bandwidth of the SPU FPGA data path. Although the PET data message sizes are up to 9 times larger than those occurring in the Hyperion I, the Hyperion II^{D} acquisition system reveals a similar stable and linear transmission behaviour to that of Hyperion I. Radionuclide-based PET measurements revealed message-header-CRC-related faults for a radionuclide activity $\geq 70\,\mathrm{MBq}$ detected at the data path inputs of the SPU FPGA. This needs further investigation to verify if header data was actually corrupted or if the module receiving the messages reveals a faulty detection behaviour at high data rates. Such radionuclide activities are typically not used for small-rodent imaging, but are not uncommon for rabbit imaging [176, 177, 178, 179]. Despite the detected faults, the acquisition platform did not show signs of blocking (or paralysing) behaviour and for lower activities, no faults were detected. Count-rate measurements reported with the system in [158, 159] with initial activities of up to 100 MBq confirm the high data rate robustness and non-blocking behaviour of the data acquisition platform. Finally, simultaneous PET/MRI measurements were performed to investigate the influence of MRI gradient field switching and RF pulse excitation with respect to data corruption due to induced noise pick-up. The measurements did not show any faults resulting from operating the MRI under severe conditions (gradient switching with steep gradient slopes and repeated TSE RF pulse excitation).
In addition to investigations related to the fault detection observed at high tracer activities, future work should address a change in prioritisation handling between PET and ctrl/status data messages by the second-stage-arbiter in the FPGA designs. This would remove the losses of control/status data messages when the acquisition architecture operates at the throughput range limit. In practice, this has not been an issue for Hyperion II^{D} considering the very low ctrl/status data message rate combined with the large sizes of PET data messages during high hit data rates. Besides a bandwidth increase of the downstream data path in

the SPU FPGA design to further increase the throughput range for hit data, steps towards FPGA-based data processing should be taken to significantly reduce the amount of data transfer during imaging. This includes FPGA-based hit pre-processing as well as singles processing.

The second aim of the thesis was to investigate, if RF interference could be reduced by making modifications to the PET acquisition platform.
While the shielding of a PET/MRI system might yield a satisfactory interference reduction for a majority of MRI sequences, some sequences used for fast or high-resolution MR imaging tend to suffer from a low SNR and or are prone to PET-related RF interference. The PET RF shields are usually a fixed part of the system design and cannot be optimised in the field. In chapter 4, it was proposed to gate the PET data acquisition and thereby reduce RF emission from PET electronics during the MRI RF reception phases. This is possible when the PET and MRI operation is synchronised and the process of entering and leaving the gate phase is shorter than the actual RF reception time used by MRI sequences of interest. A gating phase introduces a PET sensitivity loss due to the lack of data acquisition. Therefore, the overhead times for the switching process should ideally represent a small fraction of the MRI RF reception time to avoid further loss of PET sensitivity. The concept of PET acquisition gating was investigated with a single Hyperion II*D* PET module to study the noise reduction gained by switching of the DPC sensors. First, a new method was presented to quickly switch off and on the sensors so that the gating procedure could be applied. MRI noise measurements with the new quick-switching-method demonstrated its feasibility and yielded a drop of the MR noise level down to that measured with the PET module turned off. As the drawback of this technique is a PET sensitivity loss, its application is limited to the protocols where the PET acquisition time can be extended to make up for the loss in sensitivity. Future work should test the gating technique at system level by synchronising the PET with the MRI. This could be done either via the RF coil electronics or via an MRI trigger provided through MR sequences. The method via the coil electronics is easier and more flexible, as it does not require MR sequence modifications to be programmed.
Unlike the RF interference reduction techniques above, the two techniques presented in chapters 5 and 6 are applicable throughout the complete MRI sequence

execution. They are applicable to PET detectors using digital, clocked electronics and are based on the idea of modifying the RF fields emitted by PET such that the field coupling is reduced. This is achieved by a field amplitude reducing the amplitude of frequencies, the MRI receive chain is sensitive to, and by changing the spatial pattern of the RF field. The techniques are based on the adjustment of the frequency (chapter 5) and the phase (chapter 6) of the DPC sensor clock signal. This can be done solely by adjusting the FPGA firmware of the PET modules since the entire reference clock distribution of the Hyperion II$^{\mathrm{D}}$ system is controlled and distributed by FPGAs. Measurements with a spectrum analyser showed that frequency shifts of the DPC sensor clock result in amplitude variations of the RF emissions over a broad frequency spectrum. By shifting the frequency in such a way that the amplitudes are reduced for the MRI-sensitive narrow frequency bandwidth around the Larmor frequency, the coupled noised is reduced. This was successfully demonstrated with MRI spurious signal (noise) scans. The impact on the RF field distribution and amplitudes resulting from clock phase shifting was first studied via field simulations of a clock phase arrangement in the form of a checkerboard pattern. This led to field distribution changes with lower amplitudes compared to in-phase pattern clocking. The simulations were confirmed by MRI noise measurements using a single SDM where the checkerboard application led to a noise reduction of a factor of approx. 2.
The fundamental approach of the clock frequency and phase shift techniques lies in modifying the generated RF field rather than suppressing it as commonly done by RF shielding. With a combined application of these techniques, PET detectors with digital electronics could in principle be operated without or with only minimal shielding. This would reduce local MRI gradient- and B_0 field disturbances and thus help to preserve MR image quality. As the PET-related RF field emission can be changed in the field by modifying FPGA firmware, the emission characteristics could be adjusted and thus optimised to different MRI RF receive coils. In the same way, PET inserts for hybrid PET/MR imaging could be combined with MRI systems of different field strengths, thereby increasing the application range of the PET inserts. Future steps in the field of RF interference reduction are the implementation and assessment of the three techniques above on a system level, and to study their effectiveness when PET RF shielding is reduced or removed. Additionally, initial investigations should be started to obtain

a model that can predict the RF field changes resulting from modifications of the clock frequency and phase.

Chapter 7 gave an overview of PET/MR imaging results to demonstrate the *in vivo* and *ex vivo* imaging capabilities of the Hyperion II^D system which incorporates the data acquisition system described in this thesis. The high spatial resolution reported in [125] enabled mouse bone-scan images with a high level of detail of the bone structures and offered good images of the very small arteries outgoing from the murine aortic arch. The images obtained from an *ex vivo* measurement of a rabbit abdominal aorta allowed the vessel walls to be distinguished from the vessel lumen. These results are very promising for current and proposed future imaging projects in the area of cardiovascular research.

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Appendix A

Acronyms

2D	**2**-**D**imensional
3D	**3**-**D**imensional
APD	**A**valanche **P**hoto-**D**iode
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
aSiPM	**a**nalogue **S**ilicon **P**hoto-**M**ultiplier
CC	**C**reative **C**ommons
CLB	**C**onfigurable **L**ogical **B**lock
CMR	**C**ardiovascular **M**agnetic **R**esonance imaging
CMT	**C**lock **M**anagement **T**ile
CPS	**C**ounts **P**er **S**econd
CoG	**C**enter **o**f **G**ravity
CSU	**C**entral **S**ynchronisation **U**nit
CT	**C**omputed **T**omography
CVD	**C**ardio-**V**ascular **D**isease
DAC	**D**igital-to-**A**nalog **C**onverter

DACA	**D**ata **A**cquisition and **C**ontrol **A**rchitecture
DAPA	**D**ata **A**cquisition and **P**rocessing **A**rchitecture
DCM	**D**igital **C**lock **M**anager
DCR	**D**ark **C**ount **R**ate
CRC	**C**yclic **R**edundancy **C**heck
DAPS	**D**ata **A**cquisition and **P**rocessing **S**erver
DAQ	**D**ata **AQ**uisition
DDG	**D**ummy **D**ata **G**enerator
DPC	**D**igital **P**hoton **C**ounter
dSiPM	**d**igital **S**ilicon **P**hoto-**M**ultiplier
DSP	**D**igital **S**ignal **P**rocessor
EHU	**E**rror **H**andling **U**nit
EPI	**E**cho-**P**lanar **I**maging
FFE	**F**ast **F**ield **E**cho
FIFO	**F**irst **I**n **F**irst **O**ut
FPGA	**F**ield-**P**rogrammable **G**ate **A**rray
FPV	**F**loating **P**oint **V**alues
FoV	**F**ield **o**f **V**iew
FID	**F**ree **I**nduction **D**ecay
FSM	**F**inite **S**tate **M**achine
FWHM	**F**ull **W**idth **H**alf **M**aximum
GRE	**F**radient **E**echo

HDL	**H**ardware **D**escription **L**anguage
ID	**Id**entifier
ISE	**I**ntegrated **S**oftware **E**nvironment
JTAG	**J**oint **T**est **A**ction**G**roup
LCD	**L**iquid **C**rystal **D**isplay
LOR	**L**ine **O**f **R**esponse
LSB	**L**east **S**ignificant **B**yte
LSO	**L**utetium **O**xyortho-**S**ilicate
LVDS	**L**ow-**V**oltage **D**ifferential **S**ignaling
LYSO	**L**utetium **Y**ttrium **O**xyortho-**S**ilicate
Mb	**M**ega-**b**it
MB	**M**ega-**B**yte
MRI	**M**agnetic **R**esonance **I**maging
MSB	**M**ost **S**ignificant **B**yte
MTP	**M**ultiple-**F**ibre **P**ush-On/Pull-off
PDPC	**P**hilips **D**igital **P**hoton **C**ounting
PET	**P**ositron **E**mission **T**omography
PLL	**P**hase-**L**ocked **L**oop
POF	**P**lastic **O**ptical **F**ibre
PPM	**P**arts **P**er **M**illion
RAM	**R**andom **A**ccess **M**emory
RESCUE	**R**eduction of MR **S**NR degradation by using an MR-syn**c**hrono**u**s

	low-interference P**E**T acquisition technique
RF	**R**adio **F**requency
ROI	**R**egion **O**f **I**nterest
ROM	**R**ead-**O**nly **M**emory
RTU	**R**emote **T**rigger **U**nit
R&D	**R**esearch and **D**evelopment
SE	**S**pin **E**cho
SiPM	**S**ilicon **P**hoto-**M**ultiplier
SNR	**S**ignal-to-**N**oise **R**atio
SPECT	**S**ingle-**P**hoton-**E**mission **C**omputed **T**omography
SPAD	**S**ingle-**P**hoton **A**valanche **D**iode
SPU	**S**ingles **P**rocessing **U**nit
SR	**S**lew **R**ate
TCP/IP	**U**ser **D**atagram **P**rotocol/**I**nternet **P**rotocol
TF	**T**urbo **F**actor
TSE	**T**urbo **S**pin **E**cho
Tx/Rx	**T**ransmit/**R**eceive
TTL	**T**ransistor-**T**ransistor-**L**ogic
UDP/IP	**U**ser **D**atagram **P**rotocol/**I**nternet **P**rotocol
VHDL	**V**ery high Speed Integrated Circuit **H**ardware **D**escription **L**anguage