Adaptive Multi-band Rectifier System for Stabilized Wireless Energy Harvesting at Flexible Distances and Dynamic Conditions

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***Abstract*—The unpredictable propagation of ambient Radio Frequency (RF) waves may cause significant randomness in power densities against the propagation distance, time and locations. To address this challenge, we propose a novel adaptive rectifier system with stabilized output DC power against dynamic power densities. A novel detection circuit is designed to identify the frequency range and receiving power level. Then the received RF power is amplified to the saturated level by referring to the detected frequency and power information for adaptive DC biasing control for an integrated power amplifier. Doing so makes the input power to the rectifier constant regardless of the power and frequency variations. The experimentally validated system can output a stabilized power under the time-varying power range of –10 dBm ~ 0 dBm and location varying within 0.5 m at 1.8 GHz, 2.1 GHz and 2.6 GHz. Compared to conventional designs, this system has realized stabilized and enhanced conversion efficiency (61% @ 1.8 GHz, 64% @ 2.1 GHz, and 53% @ 2.6 GHz) and therefore could be adopted for wireless powering distributed sensors and IoT devices continuously and steadily at flexible conditions.**

***Index Terms*—Adaptive rectifier system, tri-band rectifier, frequency and power detection circuit, stable DC power output.**

I. Introduction

TO address acute resource and environmental constraints, reducing carbon footprint has been a major strategic decision for alleviate the energy crisis and the global warming caused by traditional mineral energy. Radio frequency (RF) power as one of the "renewable" energy sources [1-2], extremely booms in ambient environment as the prompt development of the wireless communication technology, and therefore leveraging the redundant RF energy will do favor to addressing the Net Zero 2050 target by saving the waste of batteries and power accessories.

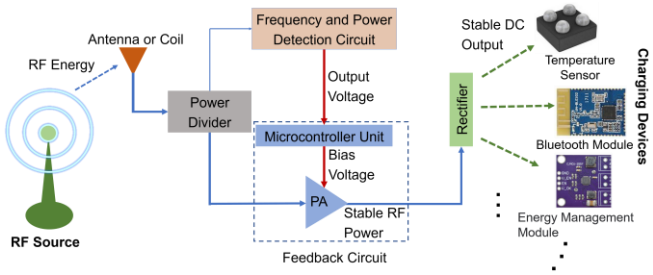

Fig. 1. Proposed radiative RF energy harvesting system using novel rectifier with an adaptive output power stability.

Regarding the RF/wireless energy harvesting, rectifier technology is by far the best option which can directly convert the received RF energy into direct current (DC) energy with high efficiency in real time [3, 4]. Nowadays, major research activity for the rectifier has been focused on improving its RF-DC conversion efficiency [5-7] as well as extending its working frequency bands [8-10] or bandwidth [11-14], and remarkable progress has been made through tireless efforts of researchers [15-17]. Nonetheless, the existing explorations are mainly based on the stable external RF energy [18-20], while the actual RF power received by antenna is dynamically varying in terms of change over time and location considering the daily electromagnetic (EM) environment [21-23], which will directly disorder the output DC power generated by the rectifier [24]. Therefore, if this rectifier is adopted to supply the battery-free devices working at the abovementioned RF energy harvesting system, the unstable output power will affect its normal operation and even damage [25, 26] it due to the possible overload. To address this problem, some attempts have been taken to overcome the limitation of the existing rectifier. For example, in Ref. [27], a power management integrated circuit (PMIC) is connected to a rectifier to make sure a long-distance Bluetooth Low-Energy (BLE) device work proper. Although the BLE can be isolated by the PMIC from the rectifier receiving dynamic RF energy, the BLE only can

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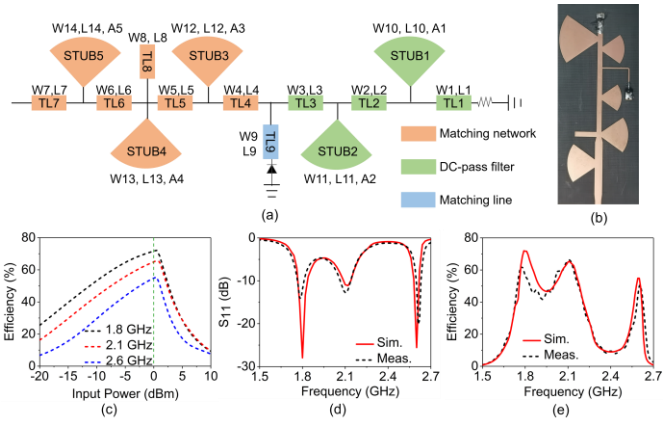

Fig. 2. (a) Topology of the proposed rectifier. (b) Fabricated prototype of the proposed tri-band rectifier. (c) Simulated RF-DC conversion efficiency of the proposed rectifier versus input power level at three frequencies for a load resistance of 2100 Ω. Simulated and measured reflection coefficient (d) and RF-DC conversion efficiency (e) of the proposed rectifier at 0 dBm for a load resistance of 2100 Ω. (W1 ~ W5, W10, W11, W12 = 1.9 mm; W6 ~ W8, W13, W14 = 2.9 mm; W9 = 0.5 mm; L1, L3 = 6 mm; L2 = 2 mm; L4, L7 = 10 mm; L5 = 11 mm; L6, L8, L11= 8 mm; L9 = 18 mm; L10 = 14.4 mm; L12 = 7 mm; L13 = 9.6 mm; L14 = 9.8 mm; A1 ~ A5 = 70^0)

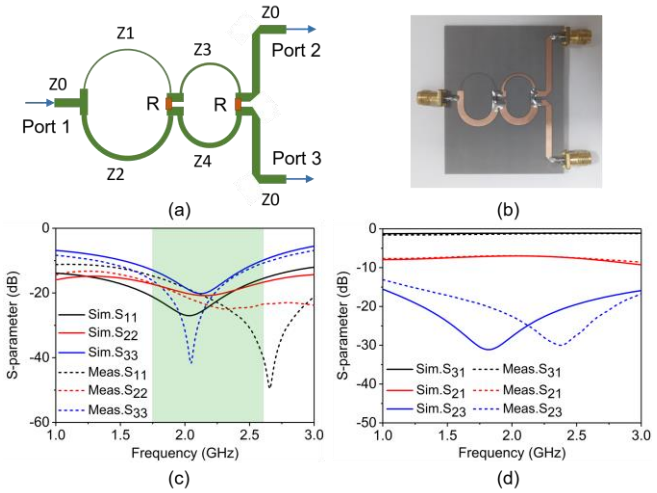

Fig. 3. (a) Topology of the proposed PD. (b) Fabricated prototype of the proposed 1:4 PD. (c) Simulated and measured reflection coefficient of the PD. (d) Simulated and measured S_{21}, S_{31} and S_{23} of the PD.

transfer data per 30-minute because the PMIC needs to accumulate enough power to wake-up the communication. Through this indirect strategy, part of the problem has been addressed but how to maintain the battery-free devices operate continuously is still challenging. In addition, considering the abundant channels [28-30], it is significantly meaningful to explore the adaptive rectifier (especially adaptive to input powers) working at multiple frequency bands, which possesses robust EM environment adaptability.

Herein, to completely solve the problem mentioned above, a tri-band (operating at 1.8 GHz, 2.1 GHz, and 2.6 GHz) Frequency and Power Adaptive Rectifier System (FPARS) (as shown in Fig. 1) is proposed to realize the input frequency and power detection for keeping the output DC power stable as the input power varies from –10 dBm to 0 dBm. As shown in Fig. 1, the FPARS is composed of four components, including a Power Divider (PD), a frequency and RF power detection circuit, a feedback circuit (containing a Microcontroller Unit (MCU) and an integrated Power Amplifier (PA)) and a rectifier. When a specified RF signal flows into this system, with the aid of the PD, minor power flows into the detection circuit for determining both the frequency and RF power of the input signal, and the major power enters the backward rectifier after being amplified by the PA to a preset stable value (that enables the highest RF-DC conversion efficiency of the rectifier). Then, a stable DC power can be output through the nonlinear process of the rectifier. The major power to the rectifier is recognized by referring to the detected minor power and the power distribution coefficient of the PD. And the insufficient power to the preset value can be supplied by using the PA with adaptive controlling of the pre-measured bias voltage. To realize adaptive modulation and automatization of the overall system, the correspondence between the output voltage acquired from the detection circuit (revealing the minor RF power) and the bias voltage required by the PA will be stored in the MCU to form a closed control loop. In the following sections, we will systematically present the four parts of the proposed FPARS, and comprehensively showcase the tested performance of the integrated system.

II. Tri-band Rectifier Design

As the fundamental component of the proposed FPARS, the rectifier (green part in Fig. 1) needs to be designed first to determine the operating frequency bands and the optimal input RF power as the benchmark for the following feedback system. To harvest abundant RF energy from highly regarded frequency bands, a tri-band rectifier is proposed for GSM-1800 (1.8 GHz), UMTS-2100 band (2.1 GHz), and 5G band (2.6 GHz), as shown in Fig. 2(a). A single shunt diode rectifier is selected for its high RF-to-DC conversion efficiency at a low input power level [31-34]. The designed tri-band rectifier consists of a diode, a matching line at the front of the diode, a tri-band DC-pass filter, a tri-band matching network, and a load. Schottky diode SMS7630 is chosen as the rectifying diode due to its low bias voltage requirements at low input power levels (forward bias voltage: 60 mV ~ 120 mV at 0.1 mA). The matching transmission line (TL9) can adjust the input impedance diode by optimizing the W9 and L9 to improve the RF-DC conversion efficiency of the rectifier. In addition, three transmission lines and two radial stubs (TL1, TL2, TL3, STUB1, STUB2) are designed to construct a triple-band DC filter. By tuning the length of the transmission lines and radial stubs, the input impedance can be adjusted to confine the fundamental frequency energy through the load. To implement tri-band rectification, the triple-band matching network is designed by utilizing triple-stub tuning (TL4, TL5, TL6, TL7, TL8, STUB3, STUB4, and STUB5), as shown in Fig. 2(a). The rectifier is simulated and optimized in the Advanced Design System (ADS) by using the harmonic-balance (HB) simulator as well as the nonlinear SPICE model of the diode (with parasitic elements). The simulated RF-DC conversion efficiency as a function of input power at the three pre-defined frequencies is depicted in Fig. 2(c). It is obvious that as the

input power level increases, the RF-DC conversion efficiency gradually increases as a function of power and reaches its peak value at the optimal power level when the output DC is close to the diode breakdown voltage (0.5 dBm @ 1.8 GHz, 1 dBm @ 2.1 GHz, and 1 dBm @ 2.6 GHz), reflecting the necessity of realizing steady DC power output. Here, 0 dBm is taken as the optimum input power for the rectifier by comprehensively considering the conversion efficiency and breakdown voltage of the rectifier. In addition, the load resistor is optimized to 2100 Ω for realizing the highest RF-to-DC efficiency across the triple bands as the input power is constraint to 0 dBm. To keep the total system illustrated in Fig. 1 always showing the best performance, based on the abovementioned analysis, the variable RF power into the rectifier will be compensated by a PA designed in the following process and fixed to 0 dBm.

To verify our design, a prototype is printed on a low-cost F4B substrate with a relative permittivity of 2.2, loss tangent of 0.001 and thickness of 0.762 mm, as shown in Fig. 2(b). The simulated and measured reflection coefficient S_{11} at the input power levels of 0 dBm is plotted in Fig. 2(d). It is obvious that the measured S_{11} is –15 dB @ 1.8 GH, –12 dB @ 2.1 GHz and –20 dB @ 2.6 GHz, indicating the good impedance matching of the designed rectifier. The RF-DC efficiency of the rectifier is also evaluated at the input power level of 0 dBm, as shown in Fig. 2(e), and the counterpart can be obtained by using the following equation:

$$Efficiency = (I_L^2 \times R) / P_{in} \quad (1)$$

where R is the optimal load resistance of the rectifier (2100 Ω), P_{in} is the input power provided by the signal generator, and I_L is the current across the load resistance. Fig. 2(e) shows that the peak efficiencies at the three bands are 61%, 64%, and 53% for 0 dBm. Comparing the measured result with the simulated one, the frequency has a small deviation, and the measured RF-DC conversion efficiency of the rectifier at 1.8 GHz is slightly lower than the simulated result due to welding errors and the inaccuracy of the nonlinear model of the diode. Despite of these discrepancies, the rectifier still exhibits high RF-DC conversion efficiency in the preset three frequency bands, which is consistent with our design target.

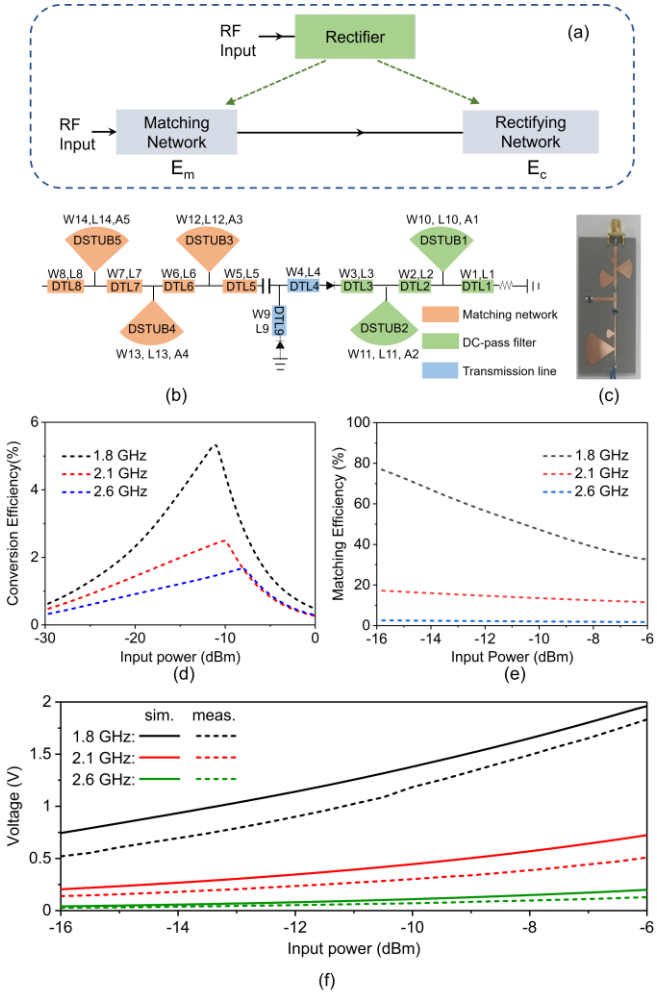

Fig. 4. (a) Configuration of a typical rectifier. (b-c) Topology and fabricated prototype of the proposed detection circuit. (d) RF-DC conversion of the designed rectifying network as a function of input power at 1.8 GHz, 2.1 GHz, 2.6 GHz. (e) Matching efficiency of the designed matching network as a function of input power at 1.8 GHz, 2.1 GHz, 2.6 GHz. (f) Simulated and measured output voltage as a function of the input power at 1.8 GHz, 2.1 GHz, 2.6 GHz. (W1 ~ W8, W10 ~ W14 = 1.86 mm; W9 = 2.2 mm; L1 = 7.7 mm; L2 = 8 mm; L3 = 12 mm; L4 = 5 mm; L5, L6 = 4 mm; L7 = 3 mm; L8 = 4.3 mm; L9 = 13 mm; L10 = 16.5 mm; L11 = 4.4 mm; L12 = 7.6 mm; L13 = 8.6 mm; L14 = 1.3 mm. A1 ~ A5 = 70^0)

III. Power Divider Design

On the basis of the predesigned tri-band rectifier, to keep the output DC power stable at the preset frequencies, the RF power into the rectifier and the detection circuit must be homologous (namely with same frequency). Therefore, to meet this requirement, a PD should be designed to link the rectifier and the detection circuit used for distinguishing the frequency and input RF power. In the meantime, considering the energy utilization efficiency, major RF power needs flow to the rectifier while relatively low power is used for the power level and frequency detection.

Based on the above considerations, a wideband 1:4 PD is proposed in this section to simultaneously meet these two demands. To achieve the wideband performance of the PD, a two-sectional Wilkinson PD structure is adopted, as shown in Fig. 3(a). The circuit is optimized using ADS software, and the characteristic impedances of each microstrip lines (Z_0, Z_1, Z_2, Z_3, and Z_4) are 50 Ω, 180 Ω, 46 Ω, 82 Ω and 43 Ω, respectively. To verify our design, a prototype is printed on a low-cost F4B substrate with a thickness of 0.762mm, as shown in Fig. 3(b). The simulated and measured S_{11}, S_{22} and S_{33} are plotted in Fig. 3(c). It can be seen that S_{11}, S_{22} and S_{33} are all less than –10 dB at the 1.75 GHz ~ 2.63 GHz, showing good transmission efficiency and small insertion loss at the three operating frequency bands. Additionally, to validate the RF power distribution performance, the S_{31} (denoting RF power from port 1 to port 3) and S_{21} (denoting RF power from port 1 to port 2) of the PD have been simulated and measured, and the corresponding data is plotted in Fig. 3(d). The measured S_{31} and S_{21} are –1.3 dB & –7 dB @ 1.8 GHz, –1.2 dB & –6.9 dB @ 2.1 GHz, and –1.2 dB & –7.6 dB @ 2.6 GHz, respectively. It is obvious that the difference between S_{31} and S_{21} in all three bands is about 6 dB, which means the output power of port 3 is

TABLE I
SIMULATED RESULTS OF THE DESIGNED DETECTION CIRCUIT

(P_i, f_j)	$Em(P_i, f_j)$	$P_i \times Em(P_i, f_j)$	$E_c(P_i \times Em(P_i, f_j), f_j)$	$Em(P_i, f_j) \times E_c(P_i \times Em(P_i, f_j), f_j)$
(P_m, f_1) (–16 dBm, 1.8 GHz)	77.8%	–17.11 dBm	3.2%	2.49%
(P_1, f_2) (–6 dBm, 2.1 GHz)	11.54%	–15.4 dBm	1.94%	0.22%
(P_m, f_2) (–16 dBm,2.1 GHz)	17.4%	–23.6 dBm	1.172%	0.2%
(P_1, f_3) (–6 dBm,2.6 GHz)	1.77%	–23.5 dBm	0.69478%	0.012%

four times that of port 2, reflecting the effectiveness of the designed 1:4 PD. In the meantime, the simulated and measured S_{23} (denoting RF power from port 3 to port 2) of the PD is also depicted in Fig. 3(d) to uncover the isolation performance between port 2 and port 3. It can be seen that the realized S_{23} is less than –15 dB at the target frequency bands, indicating the ultra-low crosstalk between the output ports. The isolation between Port 2 and Port 3, also known as S23, is primarily determined by two well-selected resistors R, each with a value of 200 Ω, as shown in Fig. 3(a). Any deviation between the simulated and measured S23 can be attributed to imperfect soldering of these two resistors during the PD manufacturing process, which cannot be directly accounted for during the simulation. Additionally, during the test process, slight welding errors in the SMA connectors can also affect the performance of the power divider.

IV. FREQUENCY AND RF POWER DETECTION CIRCUIT DESIGN

Then to adapt the different operation frequency and dynamic RF power, a frequency and power detecting circuit is necessary to supply the existing rectifier with the help of the well-designed PD. Therefore, to facilitate the synchronous detection of the frequency and RF power, a simple strategy based on the rectifier technology is put forward to distinguish the input power and frequency only by examining the output DC power.

To in-depth explain the proposed detection strategy, the input RF power (P_i) and frequency (f_j) entering the detection circuit are initially preset as:

$$P_i \in \left[P_1, P_2, \ldots, P_m\right] \text{ and } P_1 > P_2 > \ldots > P_m \left(i = 1, 2, \ldots, m\right) \quad (2)$$

$$f_j \in \left[f_1, f_2, \ldots, f_n\right] \text{ and } f_1 > f_2 > \ldots > f_n \left(j = 1, 2, \ldots, n\right) \quad (3)$$

where P_1 is less than the breakdown power and P_m is above the bias power. Only depending the output DC power $P_{out}\left(P_i, f_j\right)$ to simultaneously judge P_i and f_j, there are two problems needed to be addressed: One is for realizing the power level discrimination at the same frequency, and the other is for distinguishing frequency on the basis of solving the first problem.

As the proposed detection circuit for power-frequency multiplexing is based on the rectifier technology, a typical rectifier is carefully analyzed and deliberately designed to overcome the abovementioned two challenges. It is worth noting that for a normal operation rectifier, the output DC power (P_{out}) is positively correlated with P_i as shown in Fig. 2(c), owning to the intrinsic characteristic of the diode [35]. That's to say, the first problem can be easily solved only by arbitrarily building a rectifier because regarding to a same frequency f_j, its P_{out} is monotonically related with P_i, namely

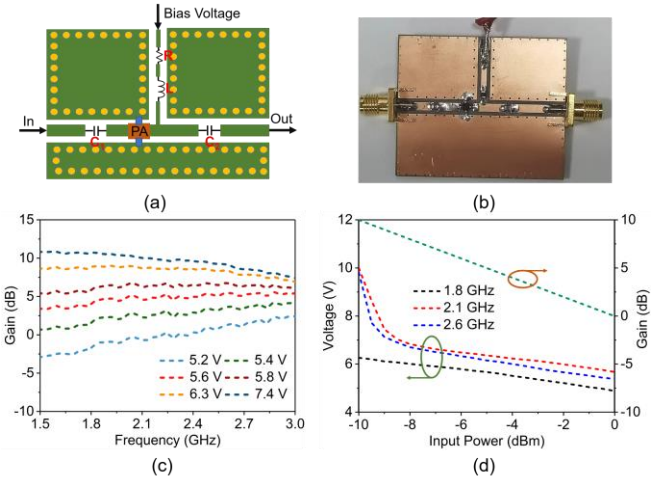

Fig. 5. Topology (a) and fabricated prototype (b) of the proposed power amplifier. (c) Measured gain as a function of the frequency at different bias voltages. (d) Required gains and the corresponding bias voltages as a function of the input power at three frequency bands.

$P_{out}\left(P_i, f_j\right) > P_{out}\left(P_{i+1}, f_j\right)$, where i = 1, 2, …, m-1. On the basis of the above conclusion, once the range of P_i is determined as Eq. (2), the output DC power range P_{out} of a rectifier operating at multiple frequency bands set as Eq. (3) can be express as:

$$\left[P_{out}\left(P_m, f_j\right) \quad P_{out}\left(P_1, f_j\right)\right] \quad (4)$$

where j = 1, 2, …, n. Hence, if any two of the above sets do not intersect, the second problem will be settled as well as the final detection circuit at the same time. It is easy to find that infinite number of solutions can be adopted to realize the non-overlapping requirements. But, if the above intervals are disordered and irregular, it will hinder the exploration of the detection strategy and summarizing the design method. Hence, considering the diode losses usually increase as a function of operating frequency [36], a monotonically decreasing manner is adopted to order the sets in Eq. (4) as

$$\begin{aligned}&\left[P_{out}\left(P_m, f_j\right) \quad P_{out}\left(P_1, f_j\right)\right] > \\ &\left[P_{out}\left(P_m, f_{j+1}\right) \quad P_{out}\left(P_1, f_{j+1}\right)\right]\end{aligned} \quad (5)$$

where j = 1, 2, …, n-1. Then, according to the transfer characteristics of the interval, Eq. (5) can be simplified as

$$P_{out}\left(P_m, f_j\right) > P_{out}\left(P_1, f_{j+1}\right) \quad (6)$$

in which P_m and P_1 denote the minimum and maximum input RF power, respectively. To further insight the design mechanism, a classical rectifier shown in Fig. 4(a) is resolved into two parts including a rectifying network with RF-DC conversion efficiency $E_c(P_i, f_j)$ and a matching

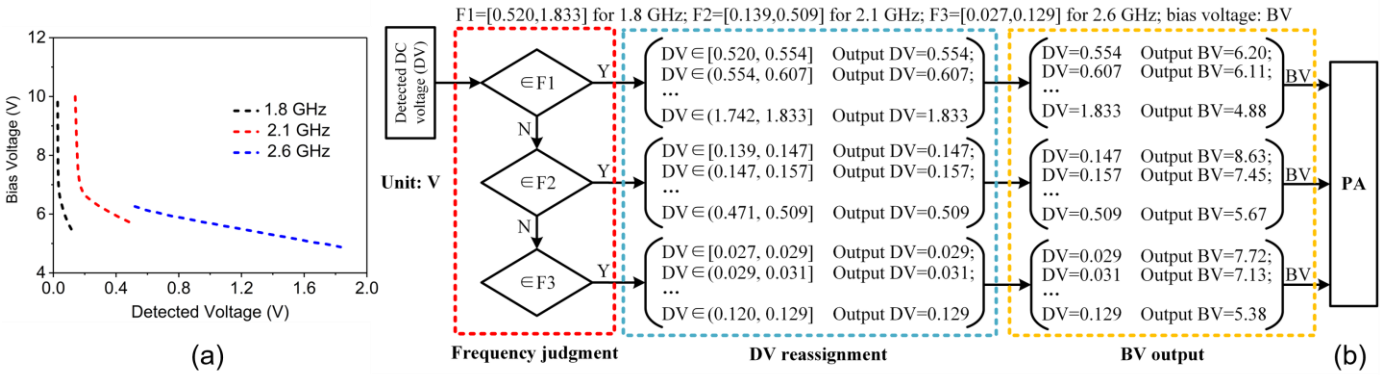

Fig. 6. (a) Corresponding relationship between the bias voltage of the PA and the detected DC voltage. (b) Control algorithm diagram of the MCU.

network with matching efficiency $E_m(P_i, f_j)$, and thereby the relation between P_{out} and P_i of the rectifier can be derived as

$$P_{out}\left(P_i, f_j\right) = P_i \times E_m\left(P_i, f_j\right) \times E_c\left(P_i \times E_m\left(P_i, f_j\right), f_j\right) \quad (7)$$

where i = 1, 2, …, m-1 and j = 1, 2, …, n. Then by substituting Eq. (7) into Eq. (6), the design principle can be finally revealed as

$$\frac{E_m\left(P_m, f_j\right) \times E_c\left(P_m \times E_m\left(P_m, f_j\right), f_j\right)}{E_m\left(P_1, f_{j+1}\right) \times E_c\left(P_1 \times E_m\left(P_1, f_{j+1}\right), f_{j+1}\right)} > \eta \quad (8)$$

where j = 1, 2, …, n-1 and $\eta = P_1/P_m$ implies the input RF power range. Eq. (8) indicates that once f_j and η are determined in advance, the detection circuit enabling dynamic frequency detection can be achieved by modifying $E_c(P_i, f_j)$ and $E_m(P_i, f_j)$ to cater to Eq. (8). In addition, due to the orderliness of the output DC power intervals (Eqs. (5) and (6)), only the maximum and minimum P_{out} at the adjacent frequency need be considered, and thereby the design difficulty can be significantly relieved as well as improving the feasibility.

So far, the design principle of the multi-band power detection circuit has been detailly demonstrated. According to this design strategy, to build a detection circuit, the frequency bands and η should be first determined based on Eq. (8). Note that the working bands including 1.8 GHz, 2.1 GHz and 2.6 GHz have been decided when we design the tri-band rectifier. In the meantime, considering the optimum input power (0 dBm) of the well-designed rectifier and the maximum gain of the following PA. The input power range for the PA is set as –10 dBm ~ 0 dBm to maintain the rectifier that can be tuned to its optimal state through external power compensation, and thereby the corresponding power detection range of the detection circuit is determined to –16 dBm ~ –6 dBm according to the power allocation ratio of the predesigned PD. Then, by substituting the frequency bands and η into Eq. (8), the corresponding requirements of the rectifying network and matching network can be derived for the following design process.

With the above determined parameters as the design target, a tri-band detection circuit is put forward, and its topology is shown in Fig 4(b). To improve the accuracy of the output voltage detection, the voltage double rectifier is used due to the high output voltage [37]. Although the abovementioned analysis is based on the output DC power, considering the load resistance of the circuit is fixed, the output DC voltage owns the almost same variation trend with the DC power. Therefore, the output DC voltage no doubt also can be used for input frequency and power detection. The designed tri-band detection circuit is constructed using a rectifying network and a matching network. The rectifying network consists of two diodes, a DC filter and a load. The Schottky diode SMS7630 is chosen as the rectifier diode due to its low bias voltage requirements at low power input levels and low losses. The DC filter consists of two radial stubs which can suppress the fundamental frequency power through the load. To increase the sensitivity of the detection voltage, the load is taken as 82 KΩ because the high load will induce high output DC voltage. The matching network is composed of a chip capacitor, three transmission lines and three radial stubs, of which the matching efficiency at three frequency bands can be adjusted by changing the length of the transmission line and the radial stub to fit the theoretical values.

In addition, the RF-DC conversion efficiency of the rectifying network (Fig. 4(d)) and the matching efficiency of the matching network (Fig. 4(e)) are extracted to verify the correction of our design. By substituting the corresponding data (Table I) into the left side of Eq. (8), the calculated results (11.3 for condition $P_{out}\left(P_m, f_1\right) > P_{out}\left(P_1, f_2\right)$ and 16.66 for condition $P_{out}\left(P_m, f_2\right) > P_{out}\left(P_1, f_3\right)$) are larger than η equal to 10, catering well for the theoretical relation expressed in Eq. (8).

Next, the simulated output DC voltages in the three frequency bands with respect to the input power are shown in Fig. 4(f). It can be seen that each output DC voltage of the detection circuit is one by one corresponding with different frequencies and input power levels. Therefore, our design can be used to pick up the input power level and frequency of the RF energy entering it only by detecting the output voltage. To further verify this detection circuit, a prototype is printed on a low-cost F4B substrate with a thickness of 0.762 mm (Fig. 4(c)), and measured. Consistent with the simulated results, the measured output voltage provided in

Fig. 4(f) is monotonous with the input RF power at the identical frequency, and no overlap can be observed at the adjacent frequencies, further verifying the effectiveness of the proposed design method.

V. Feedback Circuit Design

By now, the accurate detection of the frequency and power of the input RF signal has been achieved through the well-designed detection circuit (Fig. 4(b)). Due to the link between the rectifier and the detecting circuit by the PD, the input RF power with specified frequency flows into the rectifier can be obtained through comprehensively considering the detected power and the energy allocation ratio. Hence, a feedback circuit is needed to dynamically and adaptively compensate the insufficient power entering rectifier to 0 dBm for realizing the control system via a closed loop.

The proposed feedback circuit consists with a PA and a MCU, in which the PA works for increasing the input power lower than 0 dBm and the MCU is responsible for bridging the detection circuit and the PA. To meet the requirements for the overall system, a broadband PA covering the working bands of the predesigned rectifier is proposed based on an integrated chip (Fig. 5(a)). As the core of the PA, ERA-1SM is chosen as the PA chip, which can provide a maximum gain of 11 dB in 1 GHz ~ 3 GHz. C_1, C_2 are the isolation capacitors, taken as 1 uF, and R is the bias resistor, taken as 120 Ω. To prevent RF energy from entering the DC supply, a protective inductor L is added to the bias voltage circuit, which is taken as 10 nH. To test the actual performance of the PA, a prototype is fabricated on a low-cost F4B substrate (Fig. 5(b)). The measured gain as a function of the frequency at different bias voltages is depicted in Fig. 5(c). It is obvious that the gain of the PA increases against the bias voltage at the range of 1.5 GHz ~ 3 GHz. Based on the above rule, the gain of the PA can be manipulated by adjusting the magnitude of the bias voltage, ensuring stable power output at different input power. When the RF power into the rectifier varies from –10 dBm to 0 dBm, the required gains at three frequency bands (green dotted line) are shown in Fig. 5(d), and the corresponding bias voltages required by the PA are also provided here.

Two essential relationships, the detected DC voltage and the RF signal into the detecting circuit as shown in Fig. 4(f), and the PA required bias voltages and the RF signal into the rectifier as shown in Fig. 5(d), enable the derivation of a directly corresponding relationship between the PA required bias voltage and the detected DC voltage by the detection circuit, considering the power distribution ratio of the PD and plotted in Fig. 6(a). To close the total system loop with a simple control algorithm, an STM32 MCU is adopted, and the detection power range (-16 dBm ~ -6 dBm) is equally divided into twenty connected intervals, with the corresponding frequency-dependent voltage intervals easily obtainable from Fig. 4(f). Based on the obtained voltage boundary conditions, the MCU control algorithm comprises three modules: the first module (in the red wireframe of Fig. 6(b)) judges the input frequency information according to the frequency-dependent output voltage range ([0.52 V, 1.83 V] for 1.8 GHz, [0.14 V, 0.51 V] for 2.1 GHz, and [0.027 V, 0.13 V] for 2.6 GHz) shown in Fig. 4(f); the second module (in the blue wireframe of Fig. 6(b)) searches the matched voltage interval based on the initial detection voltage and reassigns the maximum value of this interval to the detection voltage; and the third module (in the yellow wireframe of Fig. 6(b)) determines the output bias voltage by referring to the reassigned detection voltage and the relationship shown in Fig. 6(a). The supporting information provides the detailed control codes. Once these three steps are completed, the entire system automatically realizes self-adaptive control for both input frequency and power.

VI. System Integration and Testing

Finally, to demonstrate the performance of the proposed system, the four components designed above of the total system are integrated and manufactured based on the optimized geometric dimensions, as shown in Fig. 7(a). Following, in

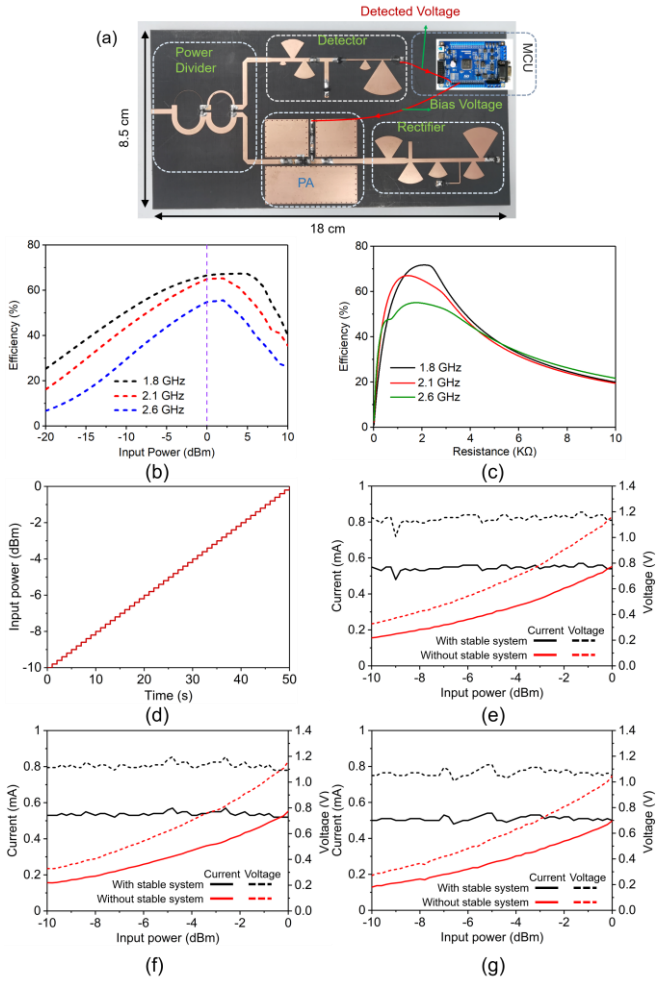

Fig. 7. (a) Fabricated prototype of the integrated system. Measured RF-DC conversion efficiency of the proposed rectifier: (b) for various input power level when the load resistance is 2100 Ω; (c) for various load resistance as the input power is 0 dBm. (d) Input power provided by signal generator as a function of time. Measured output current and voltage of the integrated system and the proposed tri-band rectifier as a function of the input power when connected to the signal generator, at (e) 1.8 GHz, (f) 2.1 GHz, (g) 2.6 GHz.

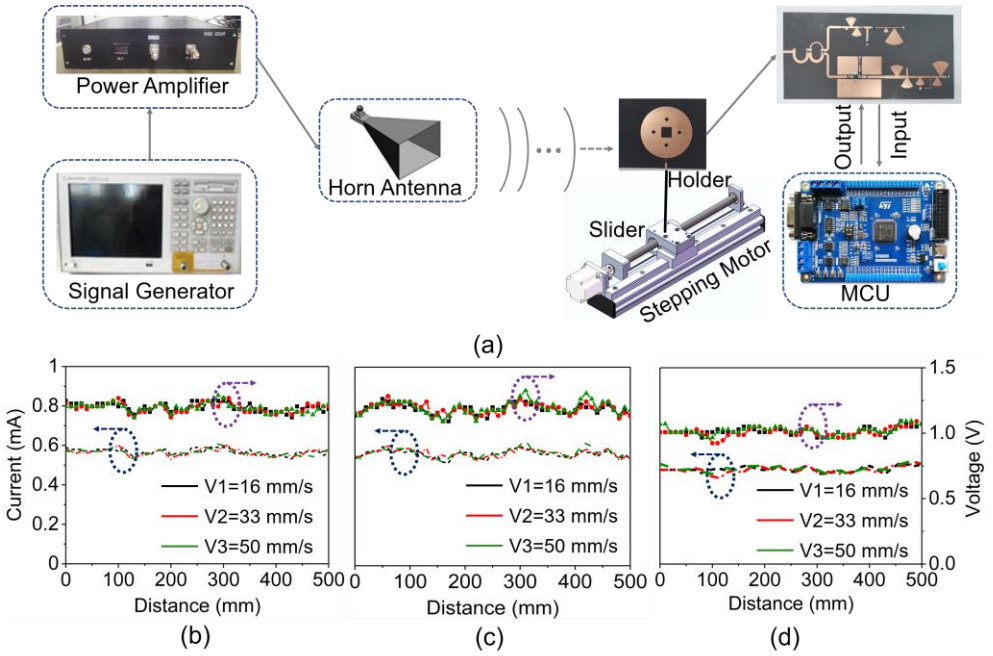

Fig. 8. (a) Measurement setup for the proposed RF energy harvesting system. Measured output current and voltage of the integrated system as a function of the distance under three speed states, at (b) 1.8 GHz, (c) 2.1 GHz, (d) 2.6 GHz.

order to verify the stability for the output DC power performance of the proposed system as the received power is dynamically varying versus time and location, the total system is separately tested for time-varying signal and location-varying scenarios. Before conducting the test mentioned above, the static performance of the rectifier embedded into the total system was analyzed in terms of the input RF power (Fig. 7(b)) and load resistance (Fig. 7(c)). From Fig. 7(b), the measured efficiency at the target frequencies gradually enhances and almost reaches the maximum value when the input RF power increases to 0 dBm, which matches well with the simulated results shown in Fig. 2(c). As the input power is increased, the diode inside the rectifier is penetrated by reverse, leading to a decay in efficiency, as predicted in Fig. 2(c) and observed in Fig. 7(b). The RF-DC conversion efficiency of the rectifier fabricated at 1.8 GHz, 2.1 GHz, and 2.6 GHz first increases and then decreases with increasing load resistance, as shown in Fig. 7(c). Although the measured efficiency is frequency-dependent, the three efficiency spectra (Fig. 7(c)) almost simultaneously reach optimal values when the load resistance is equal to the previously designed value of 2100 Ω. Given its excellent static performance, the rectifier can reliably provide high DC output under optimal operating conditions of 0-dBm input power and 2100-Ω load resistance, enabling the FPARS to operate steadily. In the following sections, we will evaluate the dynamic performance of the FPARS.

A. Testing for time varying

Here, a stepped input power (from –10 dBm to 0 dBm by 0.5 dBm per step, and each power step hold time is 1 second, shown in Fig. 7(d)) is built and put into the total system (Fig. 7(a)) to check its stable performance. Our system and a single rectifier circuit were separately connected to the signal source for comparison, and the output current/voltage was measured

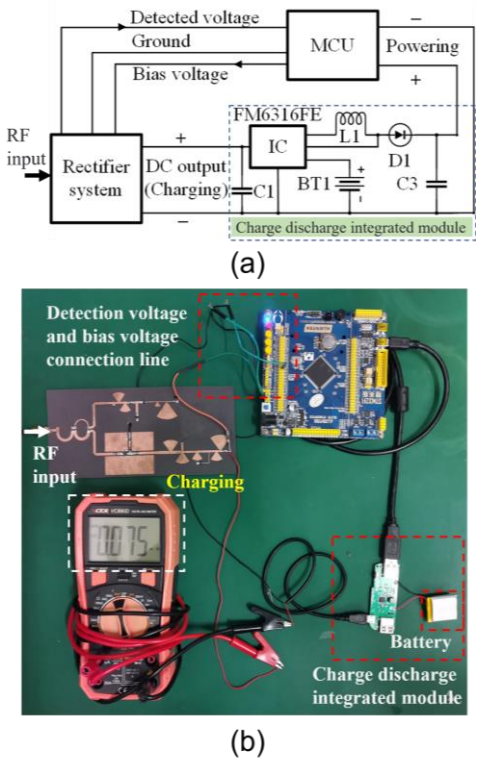

Fig. 9. Circuit diagram (a) and actual working circuit (b) for powering the MCU at actual working environment.

versus time at three frequency bands. The measured current and voltage of the FPARS and the rectifier (Fig. 2(b)) without the stable system are shown in Figs. 7(e-g). Obviously, with the increase of the input power, the output current and voltage of the rectifier increase (the test process is recorded in video 1), while the output current/voltage of the elaborately designed system is stable around 0.55 mA/1.16 V @ 1.8 GHz, 0.55 mA/1.16 V @ 2.1 GHz and 0.5 mA/1.05 V @ 2.6 GHz, proving

TABLE Ⅱ
COMPARISON OF THE PROPOSED RECTIFIER SYSTEM AND RELATED DESIGN

Ref.	Frequency (GHz)	RF-DC efficiency	Output power range as input power varying 10 dB (input power range)	Output power range versus location diversity	Output power range with time-varying input signal	Capability of keeping DC power stable
[31]	0.9	50% (–6 dBm)	–26 dBm ~ 2.3 dBm (–16 dBm ~ –6 dBm)	NA	NA	NO
[32]	2.4	58% (0 dBm)	–15.6 dBm ~ –3.8 dBm (–10 dBm ~ 0 dBm)	NA	NA	NO
[35]	1.85, 2.15, 2.45	58%/56%/50% (0 dBm)	–13.5 dBm ~ –1.7 dBm –13.7 dBm ~ 12.1 dBm –13.9 dBm ~ 12.2 dBm (–10 dBm ~ 0 dBm)	NA	NA	NO
[12]	2.45	76% (16 dBm)	10 dBm ~ 20.8 dBm (12 dBm ~ 22 dBm)	NA	NA	NO
[8]	0.9, 2.45	62%/60% (–5 dBm)	0.9 GHz: –18.8 dBm ~ –7.2 dBm 2.45 GHz: –18.2 dBm ~ –7.1 dBm (–15 dBm ~ –5 dBm)	NA	NA	NO
This work	1.8, 2.1, 2.6	61%/64%/53% (0 dBm)	1.8 GHz: –3.2 dBm~ –1.7 dBm 2.1 GHz: –2.5 dBm ~–1.7 dBm 2.6 GHz: –2.9 dBm ~ –2.1 dBm (–10 dBm ~ 0 dBm)	1.8 GHz: –2.44 dBm~ –0.97 dBm 2.1 GHz: –2.74 dBm ~–0.65 dBm 2.6 GHz: –3.55 dBm ~ –2.44 dBm (0.5 m)	1.8 GHz: –3.2 dBm~ –1.7 dBm 2.1 GHz: –2.5 dBm ~–1.7 dBm 2.6 GHz: –2.9 dBm ~ –2.1 dBm (–10 dBm ~ 0 dBm)	YES

NA: Not Available.

TABLE Ⅲ
COMPARISON OF THE DIFFERENT MCUS

	MCU in this work [43]	MCU in [44]	MCU in [41]	Commercial MCU [45]
Name	Stm32f103zet6	ATmega 256RFR2	NV-MCU	Apollo 4
Voltage (V)	2	2	1.1	1.71
Power	8 mW	9 mW	47.14 uW	96 uW
Rom (kB)	512	256	—	256
Ram (kB)	64	32	64	64
Maximum frequency (MHz)	72	16	200	96

that our design can successfully solve the influence of time-varying signals (including frequency and input RF power) on the rectification system and achieve stable DC power output (the test process is recorded in video 2).

B. Testing for Location-Varying Signal

Immediately following, to verify that the total system can overcome the spatial signal fluctuation induced by the change of the receiving locations, the proposed system was fixed on a sliding rail through a holder as shown in Fig. 8(a). During the test, the output RF power and frequency of the transmitting antenna (left side of Fig. 8(a)) were fixed, and the corresponding DC current and voltage were measured when the whole system moved along the rail with different velocities provided by a stepping motor. Enough power needed by the horn antenna (1 GHz ~ 18 GHz) was supported by a signal generator connecting with a low-noise PA (left side of Fig. 8(a)).

When conducting the testing, a receiving antenna has been adopted to catch the incident EM waves and transmit it to the backend FPARS. The output DC current and voltage shown in Figs. 8(b-d) were measured as the stepping motor was set to three different speeds (16 mm/s, 33 mm/s, and 50 mm/s). All the experiments sharable used the same distance of 0.5 m of which the corresponding path loss is approximately equal to –8 dB as needed. Figs. 8(b-d) reveal that the output current/voltage ranges are 0.52 mA ~ 0.62 mA/1.09 V ~ 1.30 V @ 1.8 GHz, 0.5 mA ~ 0.64 mA/1.05 V ~ 1.34 V @ 2.1 GHz, and 0.46 mA ~ 0.52 mA/0.97 V ~ 1.09 V @ 2.6 GHz, respectively. (the test process is recorded in video 3) Although a little difference with the measured result of the composite circuit is shown in Figs. 8(b-d), the whole system still displays stabilized output DC power against remote distances and dynamic conditions, indicating the feasibility of the proposed FPARS.

During the measurement process described above, the load resistor had to be embedded into the total system to evaluate the system's overall performance. To power the MCU when the load resistor was replaced, an external DC source was used. However, since the MCU has a high-power consumption (0.75 W), which is more than our output power, the RF power alone was not sufficient to power it. To address this, a charge-discharge integrated module (shown in Fig. 9(a)) was used to partially power the MCU with the system's DC output and an additional DC source. The module is based on a portable electricity source management chip (FM6316FE). A corresponding powering test was conducted and shown in Fig. 9(b), with the detected current indicating that our system can directly charge the charge-discharge integrated module. Under this power supply condition, the MCU can operate properly. It is worth noting that this situation can be improved in the following two ways:

1) The proposed system can be applied to high-power wireless power transfer (WPT) applications, where the rectifier can output DC power higher than 0.7 W [38-40],

TABLE IV
COMPARISON OF THE PROPOSED SYSTEM AND RELATED DESIGN

Ref.	Communication requirement for control	Step response speed	Fixed frequency or power requirement for transmitter	Circuit complexity
[46]	RF module (2.4 GHz)	N/A (Long RF latency)	Not required	Complexity
[47]	Bluetooth	N/A (Long RF latency)	Not required	Complexity
[48]	Not required	100 us	Yes	Complexity
This work	Not required	14 us	Not required	Simple

and up to 4 W has been reported in [38]. This amount of power is sufficient to power the MCU without the need for an external DC source.

2) Alternatively, if the STM32 is replaced with a low-power MCU [41-42], the MCU controller can also be solely powered by the system. In Table III, we provide a list of these alternative low-power MCUs, including commercial options like [45] and the latest research on low-power MCUs [41]. Additionally, other low-power commercial MCUs, such as RL78/G22 [49] and STM32U5 [50], can be also applied to the proposed system. Readers can choose to replace the MCUs mentioned in this article with the low-power MCUs mentioned above based on their specific requirements.

VII. CONCLUSION

A tri-band input power adaptive rectifier system has been presented theoretically and experimentally. By analyzing and designing the power detection circuit and feedback circuit, the proposed system can achieve the aim of generating stabilized output DC power. The experimental results showed that as the input power varied with time, the composite circuit of the proposed system could continuously output the stable DC power. Further, the whole system also exhibited stable output DC power capability when the receiving power dynamically varied against the location. Compared to existing research (shown in Table II) where the rectification efficiency is heavily dependent on application conditions (e.g., power, distance, time, location), the proposed FPARS has demonstrated outstanding performance through innovative ideas and solid experimental validations, thereby becoming a transformative rectifier system for unremitting and steadying charging small electronics for real-world Internal of Things. Note that the proposed multi-band FPARS and the adaptive power control could also be exploited for low frequency (e.g., 6.78 MHz and 13.56 MHz) rectifier design for inductive WPT. Additionally, our method is distinguished by an advanced detection-control integrated system that directly correlates the detected voltage with the required bias voltage of the PA (as shown in Fig. 6(a)), without the need for extra communication between the transmitter and receiver. Although the proposed system requires an additional MCU and feedback loop, the control signal is generated in a low-cost and simplified manner, and the feedback is directly targeted at the receiving circuit. Compared to existing adaptive systems with control methods (as shown in Table IV), the proposed design demonstrates significant technical advancements in terms of simplicity and cost-effectiveness.

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